

Forethought Products

KIMSI

Interface/Motherboard

**Assembly/Operating
Manual**

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APPLICATION NOTES

ASSEMBLY INSTRUCTIONS FOR KIMSI

Introduction

Welcome to the growing group of people who are using micro-computer systems in business, control, research, and hobby applications. If you are new to electronic kit assembly, we would like to quote the best line of advice we can give you: "If all else fails, read the instructions." We know how exciting it is to be putting together a computer system, but a few minutes spent to carefully read and study the assembly suggestions can save you much frustration while you assemble a kit. Don't try to make the assembly more complicated than it is. If each component is properly soldered to each copper pad on the board, the unit will function perfectly. Just take your time on each solder joint, and everything will go smoothly.

If you need more help or clarification on how to perform some part of the assembly, don't forget your friends or acquaintances who have put together kits before. Your local computer store or computer club usually has someone with experience who is happy to help. If all else fails, drop us a note or give us a call. We're here Monday to Friday 10-6 (West Coast Time) at (503) 485-8575. This phone rings at a residence on weekends so you can usually catch us on Saturday and Sunday too.

Tools

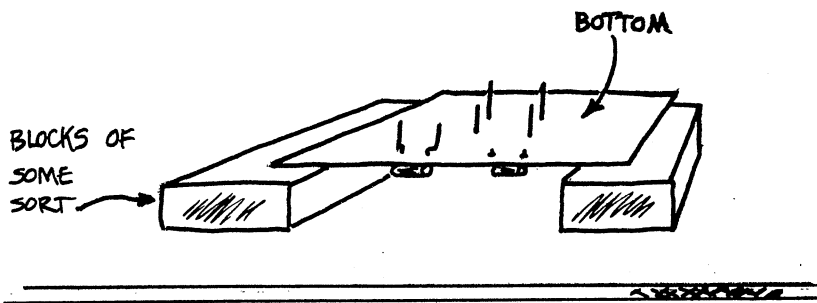
There are a few tools that are necessities for electronic assembly. They are: small screwdriver, diagonal cutting pliers (diagonal wire cutters), and wire stripper (inexpensive adjustable type). You'll need a soldering iron rated 25-42 watts. Irons with elements larger than 42 watts get too hot for heat-sensitive integrated circuits (ICs). A 25 watt unit is recommended as it is difficult to do damage to components with this heat range. The 42 watt types work fine, but should not be left on an IC pin for longer than 4 or 5 seconds at a time. The 42 watt types may be used with the very small "micro spade" tips. This tip will transfer heat from the iron to the solder joint more slowly than the regular size tips. A 1/8" round or flattened tip is usually used, and be sure to get the "long-life" or "iron-clad" type. Copper tips dissolve while you solder; they're not worth using. When you buy solder, be sure it's "rosin core"; acid core is useless (and damaging) in electrical work. It's usually best to get the smallest (finest) size of solder available. With small solder, you'll have better control over the amount of solder that is applied to each joint. If you run across "multi-core" solder, buy it, it's great.

When you get carried away and end up with too much solder on a joint, a roll of "Solder-Up" de-soldering wick will come in handy. You'll also need a slightly damp sponge to keep your soldering tip clean. A magnifying glass (up to 3X) is helpful

to see what's really happening between those little copper lines.

Work Area

A brightly lit area or a good desk lamp is essential. You may also want to find several books, wooden blocks, etc. Placing these under each end of the board will help the components from being bent when turned over for soldering.



Clothing

You may have heard of MOS or CMOS ICs that are damaged by static charges that can build up on you or your equipment. The Kimsi board uses only TTL ICs which are not sensitive to static charges. Now's your chance; put on that Hawaiian shirt made out of 12 different synthetic fibers!

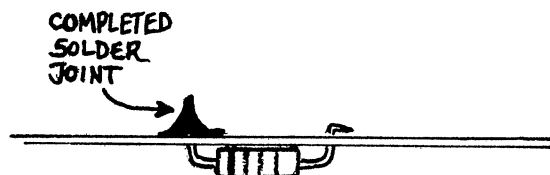
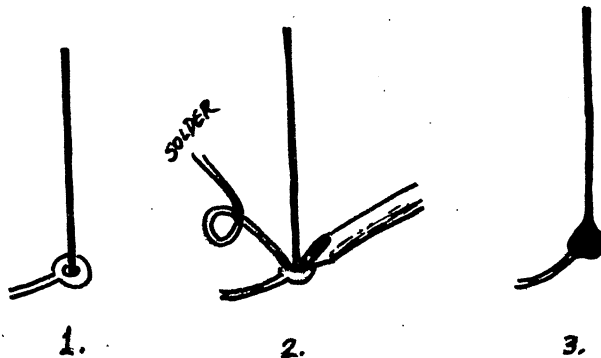
Soldering Technique

The key to good solder joints is even heating of the two metal surfaces which are being soldered together. The most important part of the process is a clean, tinned soldering tip. If the tip is not cleaned it will get a small film of corrosion over it. This outer covering does not conduct heat. A dirty tip which is pressed against the surface to be soldered will not properly heat one or both of the surfaces.

To properly clean a soldering tip, wipe it against a slightly damp sponge and immediately apply a small amount of solder directly to the tip. Applying this coating of solder to the tip (called "tinning" the tip) slows the process of oxidation

(or corrosion) and helps to conduct heat to the solder joint. The oxidation occurs while the iron is waiting to be used, so CLEAN AND TIN THE TIP JUST BEFORE USE, NOT WHEN IT IS BEING REPLACED IN ITS STAND.

To heat a solder joint, press the tip simultaneously against BOTH surfaces to be joined. Then melt the solder onto one of the metal surfaces, not onto the soldering tip. Feed enough solder onto the joint to completely cover the copper pad and form a mound around the wire or IC pin. Remove the solder and keep the iron tip on the joint for another second. This bubbles out any rosin left in the joint.



If the surface of the solder turns dull when it cools (1 to 3 seconds after removing the soldering iron), the joint was not properly heated. Apply the soldering tip to the joint and reheat it for several seconds. A small bit of fresh solder can be added since the rosin core helps the solder flow over the joint. If you get too big a "blob" on the joint, place a piece of "Solder-Up" over the joint and hold the hot iron tip on the braid until the solder is soaked up. You may have to move to fresh braid to remove all the solder on the joint.

While you are soldering you must also watch for solder "bridges." A solder bridge is a piece of solder that has stuck to a nearby copper trace and formed a bridge to another trace. This usually happens when too much solder is applied to a joint and overflows to a nearby trace or pad. It can also happen when a tinned iron is accidentally touched to the board between two or more traces. A small piece of solder can be left behind which shorts the traces together. It should be noted that soldering normally leaves a shiny transparent film of rosin behind on the board. It is not conductive, and doesn't have the silver color of solder. If in doubt, use a sharp-pointed object to scrape between the traces; rosin will scrape away, solder won't.

Remember to keep the tip clean and tinned. Give the tip an extra coat of solder before you unplug the iron and it will be easier to tin the next time you use it.

Assembling Kimsi

The top side of the Kimsi board can be identified by the "KIMSI" and "FORETHOUGHT PRODUCTS" lettering. The bottom side is covered with a dark green "solder mask" material which covers the copper traces and helps prevent solder bridges. All parts are inserted from the top of the board and soldered to the bottom side of the board. Refer to the parts placement diagram for parts location.

IC Sockets. The IC sockets which are included have one of the inside (recessed) corners molded at a 45° angle instead of a regular 90° corner. This mark is used to mark the IC pin 1 location. It aids in proper orientation of the IC during insertion.

Being careful to orient the pin 1 mark of each socket to the left (see parts placement diagram), insert 14-pin sockets for IC 1, 9, 11, 8, 10, 12, and 14. Insert 16-pin sockets for the remaining ICs. To hold the sockets in place for soldering, place a flat piece of wood on top of the sockets and tape the wood to the circuit board (so the sockets are sandwiched between the wood and the circuit board). Alternately, masking tape can be placed over each socket to hold it in place. Be sure each socket is held tightly against the board; then flip the board over and solder each pin to its pad on the bottom side of the board. Watch out for bent under pins.

R1. R1 should not be pressed tightly against the board but should be mounted with 1/8" or more of space below it. Allowing this air space, install the resistor, clip the leads, bend them to the pads, and solder.

C1-C2. C1 and C2 are polarized capacitors. They MUST be inserted with the end marked "+" connected to the circuit board pad marked "+". Insert C1 and C2, clip leads, bend to pads and solder.

C3-C10. These disk capacitors should be mounted as close to the board as possible. Insert C3 thru C10, clip all leads, bend to pads, and solder.

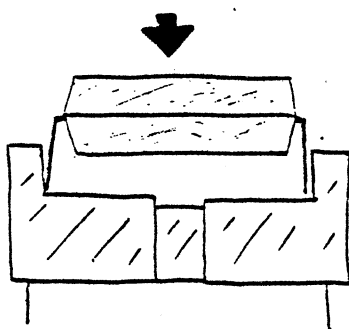
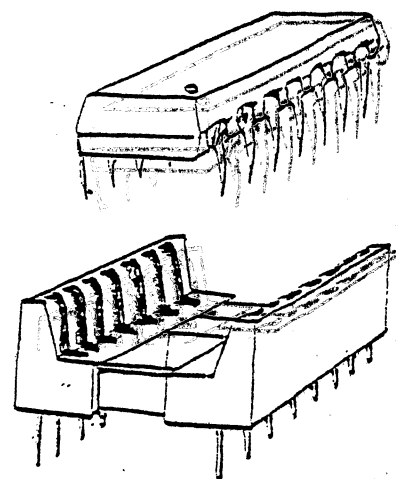
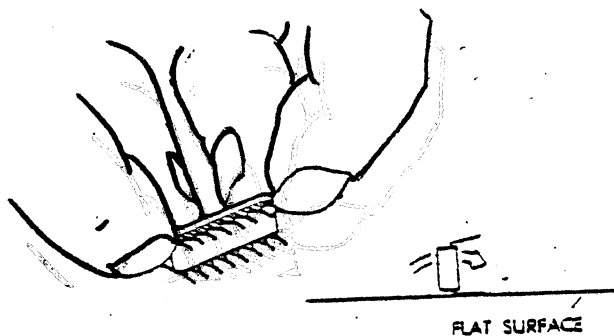
Z1. This zener diode should not be installed tightly against the board. Allow at least 1/8" of air space between Z1 and the board. Insert Z1, making sure to orient the painted band to the right as shown in the placement diagram. Clip leads, bend to pads, and solder.

Voltage Regulators. The VR1 and VR2 have two leads which are purposely off-center. All the holes will not line up properly unless the VRs and heat sinks are turned in the right direction. Place one of the VRs in a heat sink and then onto the board. When everything lines up, drop a screw in each end and attach the nuts on the bottom of the board. After both VRs are installed, solder the four leads to the bottom of the board and clip off any excess.

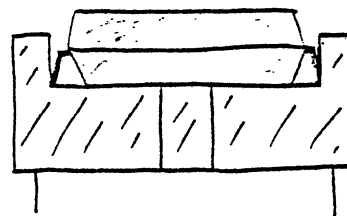
IC Insertion. ICs are usually stamped with two numbers as well as the manufacturer's initials or symbol. The first number (often on the upper part of the chip) is the date code. It is three or four digits long and tells the date of manufacture.

The second number is the type code, which identifies the function that the chip performs. This number is four or five digits long, usually ends with "A" or "N" and is surrounded by other letters which can be ignored.

Each IC is inserted by referring its type number to the Parts Placement Diagram (see IC1 is a 7420 type IC). Each IC has a mark to identify its "pin 1" (see Parts List). Pin 1 of each IC MUST be pointed toward the left edge of the circuit board (toward the heat sinks). ICs are shipped with their pins bent slightly outward. Inserting the IC will be easier if it is placed on its side (against a flat surface) and "rolled" slightly to bring each row of pins into a 90° angle with the IC body. After inserting all the ICs, recheck that each is in its proper position and is oriented toward the board's left edge. Also check to see that no pins are outside the socket or bent underneath the IC. Pins bent underneath are very hard to spot, so look closely for this.



IC being inserted
into socket

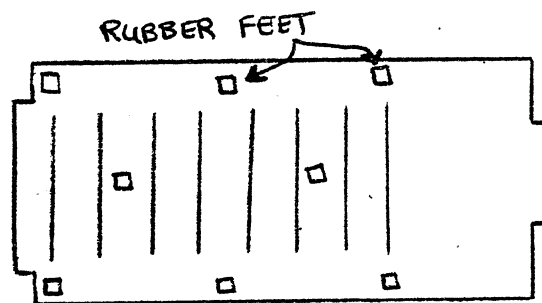


IC inserted
into socket

100 Pin Connectors. The 100 pin connectors may be placed in any configuration that is convenient. If you're not installing all eight connectors to begin with, you may want to skip every other slot, etc.

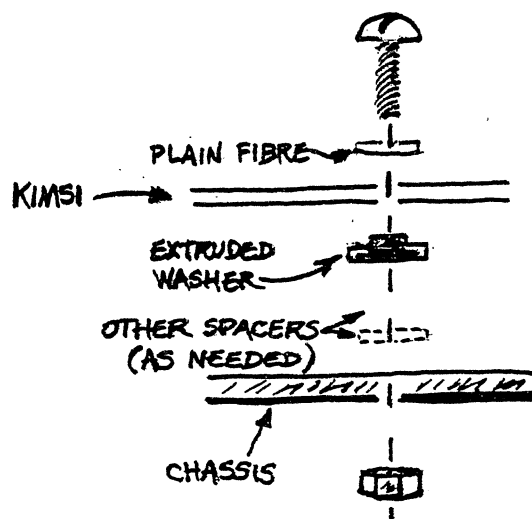
Insert the connector in place and MAKE SURE IT IS FIRMLY SEATED against the board. A connector that is soldered in place crooked is all but impossible to fix. Turn the board over and solder each pin to the board. After soldering, check carefully for solder bridges.

Mounting. Kimsi may be used with "stick-on" rubber feet or with #6 machine (or wood) screws for mounting on a base, chassis, or enclosure. For best placement of the rubber feet, follow the diagram below.



If you're mounting the board with screws, use flat and extruded washers at each mounting hole to insulate the board from the screws. Extra washers may be needed to prevent the connector pins from touching the metallic surface of the enclosure. A set of washers is available at no cost from Forethought Products (include a return envelope with your request).

This mounting may also be used with wood or sheet metal screws.



KIMSI PARTS LIST

C1-C2 22 uf/15V electrolytic capacitors

C3-C10 .1 uf disk capacitors

IC1 7420

IC2-IC4 8T97

IC5-IC7 74367 or 8097

IC8 7427

IC9 7404

IC10 7474

IC11 7400

IC12 7402

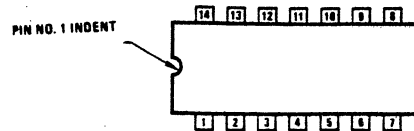
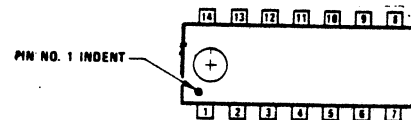
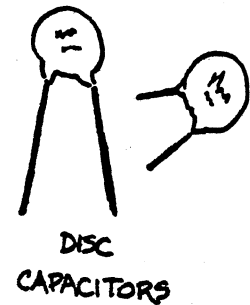
IC13 74367 or 8097

IC14 7410

R1 220 Ohm ½ watt resistor (red, red, brown).

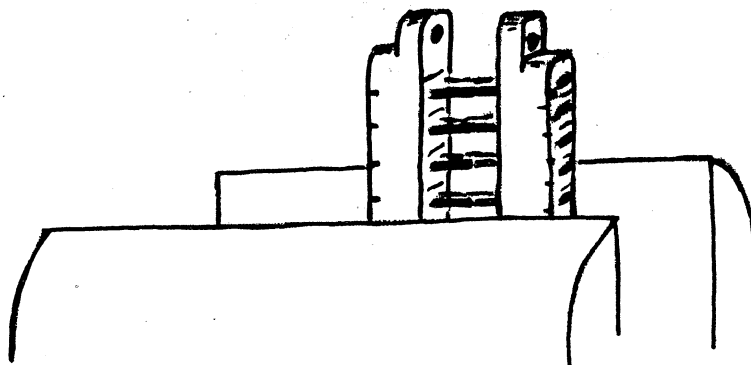
VR1-VR2 LM 309-K 5 volt regulator

Z1 1N4742A 12 volt, 1 watt, 5% zener

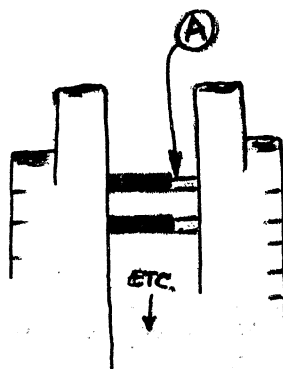


"Back to Back" connector assembly. The 44PB-K is easy to assemble since the 44-pin connectors which are provided in the 44PB kit have long solder-tail posts which form a nice fit when placed back-to-back.

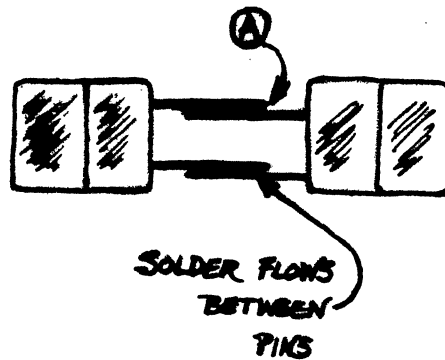
To assemble, place the two connectors into a vise as shown below.



The connectors should be pulled apart slightly so that solder will flow between the overlapping contacts.



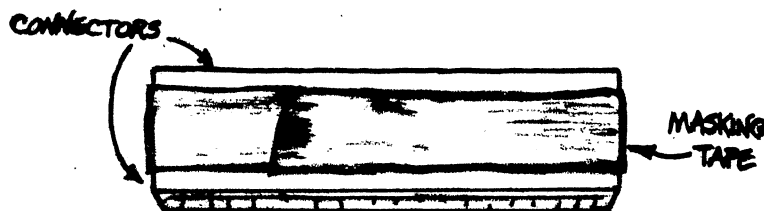
Heat the joint and apply solder at point "A". This will allow solder to flow between the two contacts as well as on top of them.



Be sure to apply enough solder so it flows between the contacts.

You may wish to do this work with the connectors lying horizontally rather than vertically as they are held in a vise. You may solder one or two joints at each end of the connector (to hold the connectors in alignment) and then remove the pair from the vise. Place the assembly on your table and solder the remaining pins together. To hold the assembly still while soldering, you can use pliers, a hammer, etc. as a weight, or else push one of the connectors onto Kimsi (do not attach the connectors to KIM while soldering as KIM is susceptible to damage by static charges).

The assembly can be "finished" with a strip of tape between the connectors.

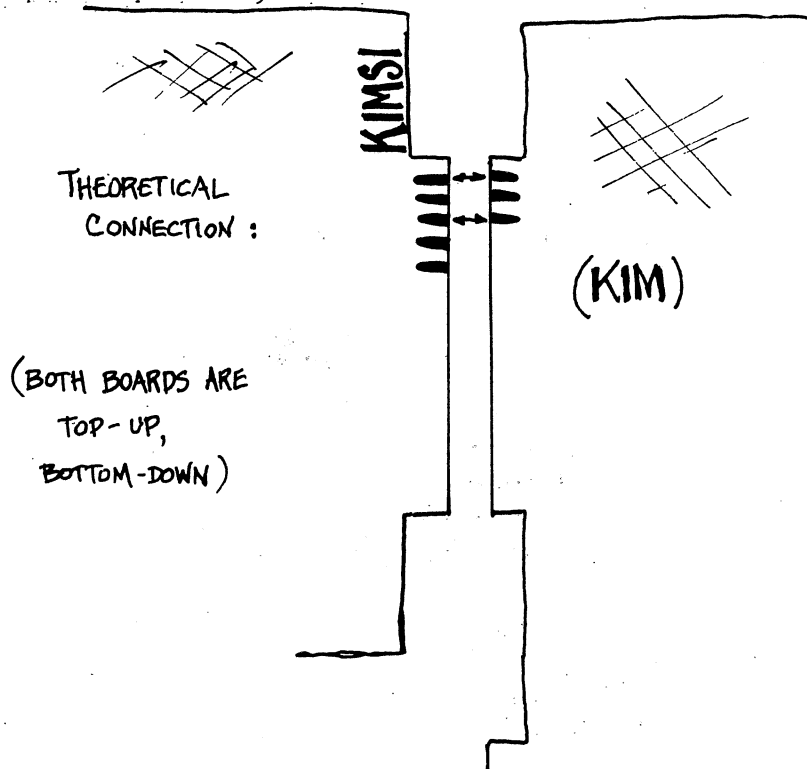


KIMSI OPERATING INSTRUCTIONS

Connecting KIM to Kimsi

CAUTION: The Kimsi board supplies regulated power (GND, +5 and +12) to KIM thru the expansion connector. Before connecting Kimsi to your KIM, remove all power connections that have been made to the application connector. In addition, remove the connection to the "decode-enable" line- "K" on the application connector.

KIM connects directly to Kimsi thru the "expansion" connector. The connector finger pattern on Kimsi is a mirror image of the KIM expansion connector. So, if you set the KIM and Kimsi next to each other as shown below, you could solder a wire from each pad of the Kimsi connector to each pad of the expansion connector (top and bottom).



A better way to do this is with two 22/44 pin (dual 22 pin) connectors soldered "back-to-back" (further information on constructing connectors can be found in the Assembly Instructions).

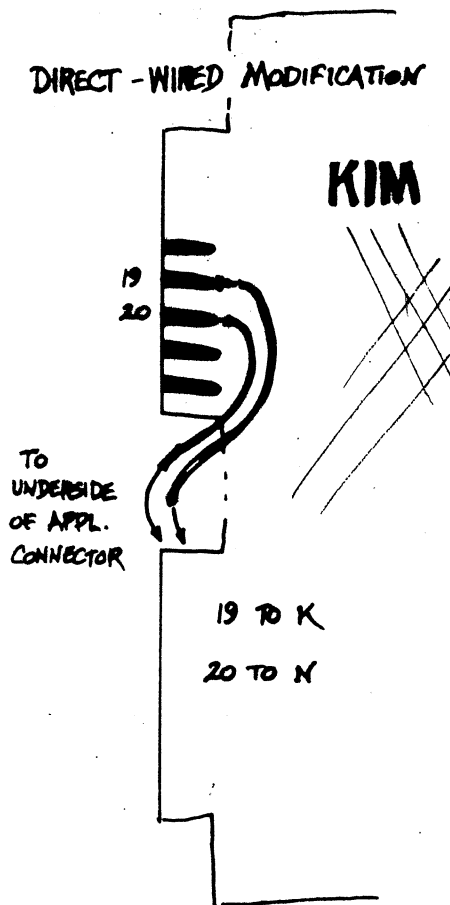
It's easy to attach KIM to one end of this connector, and Kimsi to the other, and they will come apart easily for transporting, etc.

After the expansion connector is hooked onto Kimsi, there are two other wires which must be routed to the application connector. These are the "decode-enable" signal, and the +12V supply for the cassette interface. There are three ways to do this, as listed below.

1. This is the "nicest" method, but requires soldering onto the KIM board. The "decode-enable" line and +12V line are brought out from Kimsi to pins 19 and 20 of KIM's expansion connector. These pins are empty, unused pins which have no connection to any part of KIM. These two pins (or "fingers") may be directly soldered to their destination in the applications connector with two small pieces of wire. This "modification" will not affect any past or future use of KIM, as these fingers are normally left open.

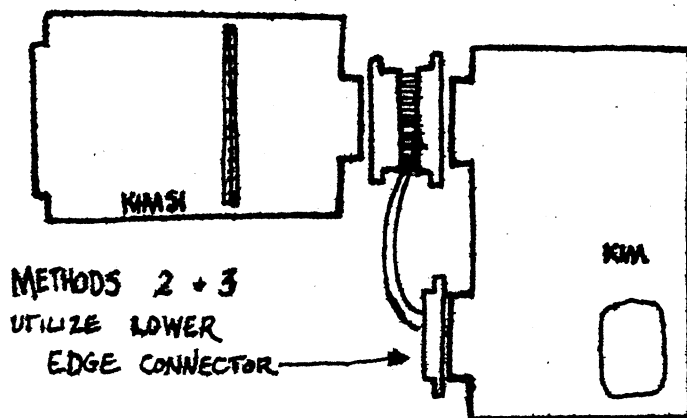
Expansion Connector to Application Connector

19	-	K
20	-	N



Methods Two and Three make these connections to the 22/44 pin connector which will attach to the application PC connector.

2. Simply attach a wire to terminal 19 on the expansion connector and connect the other end to terminal K on your application connector. Do the same for expansion connector pin 20 to applications connector pin N.



3. If it is more convenient, terminals K and N may be soldered directly to the labeled holes on the Kimsi board.

Connecting the Power Supply to Kimsi

Since Kimsi provides power to itself, KIM, and boards that are plugged into the bus, the only power supply connection necessary in the system is to Kimsi. Kimsi, when attached to KIM, requires a source of unregulated voltage approximately +8 to +10 Volts @ 2 amps. If the cassette interface is going to be used, +15 to +22V @ 200 ma is needed also. The required amount of current (amps) will increase as boards are added to the system (a 4K low power memory board draws approximately 750 ma (.750A) on the +8V supply). In addition, some board may require a negative voltage, in which case connection must be made to the "-16 Volt" pad on Kimsi.

Power supply connections are made by soldering directly to the areas on Kimsi which are marked "GND," "+8 Volts," "+16 Volts," and "-16 Volts." If alot of current is used, i.e. many boards are added to the system, be sure to use heavy wire (#10-14) for the ground and +8V lines.

Power-up

Before connecting S-100 boards to Kimsi, it's a good idea to check the operation of KIM alone. Double check the power connections to Kimsi, connect Kimsi to KIM's expansion connector, and make connection to applications connector pins K and N. Turn on the power supply and press "Reset" on KIM's keyboard. If KIM's display doesn't light, turn off the power. Check that the Decode-Enable signal present at expansion pin 19 is properly connected to applications pin K. To check the +5 power to KIM, disconnect KIM from Kimsi and connect a voltmeter to Kimsi pins 1 (GND) and 2 (+5), on the top left of the connector. Apply power to Kimsi and read 4.75 to 5.25 volts. With the voltmeter negative lead connected to pin 1, the positive lead can check the on-board regulator at IC7 pin 16. Problems with the voltage regulators (VRs) can usually be traced to unsoldered VR leads (VRs cold), untightened screws (voltage high, VRs cold), shorted (solder bridged) power traces on the board (VRs hot), or defective VRs (voltage incorrect or zero, VRs cold).

After successfully lighting KIM's display, test KIM's cassette interface. Possible problems include +16 volt supply not correctly connected to Kimsi, missing connection between expansion connector pin 20 and applications connector pin N, unsoldered leads on R1 or Z1, painted band on Z1 installed pointing wrong direction, and improper connection of audio cords to the applications connector.

Connecting S-100 Boards

All S-100 boards plug into Kimsi with their component side forward (toward the Kimsi interface section). It is best to insert them by grasping the lower corners of the board and

pressing into place (pressure on the top of the board can be disastrous if you slip).

NEVER add or remove a board from the bus with the power on. Damage can result to the board being inserted or removed. If a board doesn't seem to work, cut the power and try reinserting it into the slot. Boards can function improperly if they are not correctly "seated" into the connector.

KIM Operation with Kimsi

Kimsi has been engineered so as not to disrupt the operation of KIM in any way. The system is started as usual using the reset key and entering the stop vector. KIM will return to its monitor via reset, stop, INT or NMI (with proper vectors). The S-100 boards which are plugged into Kimsi are accessed in the same manner as the memory which resides on the KIM board. Data may be examined or changed at any location in the system using the KIM keyboard (with the exception of some I/O boards). In addition, the boards on the S-100 bus may control the CPU thru use of RDY, INT, NMI and communicate directly with each other using direct memory access (DMA).

System Map

The Kimsi board, to work properly with KIM, must reserve several areas for specific use. Boards on the S-100 bus may not be addressed at the locations reserved for use by KIM. These locations are: 000-1FFF and F000-FFFF (hex). This includes KIM's on board RAM (000-0300), I/O and ROM (1700-1FFF) and restart/interrupt vectors (FFFA-FFFF). Thus S-100 boards may be used at any address between 2000 thru EFFF.

Using S-100 RAM Boards

Random access memory (RAM) cards used with Kimsi are restricted only in that they must have an access time of 450 ns (or less) and should be static (not dynamic) type memory. Most S-100 RAM boards meet both of these requirements. Also, if 2102 type memory is used, it is advisable to purchase the low power type to help prevent a strain on your power supply as your system grows. S-100 RAM boards may be used at any location in your Kimsi system (between 2000 and EFFF) by setting the jumpers or DIP switch provided on the RAM board. S-100 RAM boards which are plugged into Kimsi are used in the same manner as KIM's on-board memory. They can be examined/ changed /saved /loaded using KIM's keyboard or cassette routines.

Using S-100 Bus ROM Boards

Read only memory (ROM) boards may be plugged into Kimsi and read in the same manner as RAM boards. Many programmable ROMs (PROMs) have an access time of 1 us (1000 ns) or more. This is nearly double the 500 ns access time required by KIM. These boards usually provide a "wait state" option which will request an extra clock cycle before attempting to read the data from the PROMs. This option essentially slows the processor down to the 1 us access time whenever it reads from the slow PROMs. This option is fully implemented on Kimsi and will work with S-100 boards which use this feature. Note that the 6502 processor may only be slowed during read cycles and not during write cycles. Thus ROM boards may use slow devices but RAM boards must meet the 500 ns access requirement.

Using S-100 Bus I/O Boards

Most input/output (I/O) boards for the S-100 bus may be used with Kimsi without modification. These include parallel and serial ports, digital to analog (D/A) converters, A/D converters, joystick interfaces and controllers for disk, tape and other storage mediums. I/O boards on the S-100 bus do not respond to a memory address as the PIAs on KIM do, but have a "port" number which is two hex digits long. This results in a maximum system capacity of 256 input (00-FF) and 256 output (00-FF) ports. Each 8 bit port is used with an IN (input) or OUT (output) instruction from the 8080. These instructions either read into the accumulator or write from the accumulator an 8 bit word at the selected port number.

When S-100 I/O boards are used with Kimsi, the port number for each board is selected (via its DIP switch or jumper) in the normal manner, but since there is no IN or OUT instruction on the KIM, another method must be used. KIM may access these I/O ports by using the special location FOXX. The memory location FOXX (where XX is a port number from 01-FF) has been reserved for use as the IN and OUT commands. A LDA F001 command will read the data from input port 01 and place it in the accumulator. Similarly, a STA F0A5 command will write the contents of the accumulator to port A5. Note that there may be both an input and an output port with the same number. Access to each port is determined by both its number and the instruction used (LDA or STA). Access to I/O ports thru address FOXX does not delay the processor in any way. The KIM keyboard can read data from an input port but cannot write data to an output port.

Note: Kimsi differs from the 8080 bus in that the 8 bit I/O port number appears only on the lower eight address lines during an I/O instruction. In 8080 systems, this eight bit number is duplicated and appears identically on both the upper eight and lower eight address lines. I/O boards may watch either A0-A7 or A8-A15 (along with I/O status lines) to determine if they are selected. Whether the upper eight or lower eight lines are used is up to the designer of the I/O board. The designer uses the set of lines which is most convenient.

I/O instructions issued through Kimsi in the form LDA FOXX activate the I/O status lines and put the port number (XX) on the lower address lines only. If you run across an I/O board which will not operate with Kimsi, take a look at its schematic. If it connects to address lines A8-A15, then it must be used at one of the seven I/O ports which are reserved for upper address line I/O. These ports are: F2, F4, F6, F8, FA, FC and FE. To use these ports, issue the instruction LDA FZ00 or STA FZ00 (where Z = 2, 4, 6...E).

In trying to keep as much standardization as possible between Kimsi systems, the I/O ports below are recommended for the following uses:

FC00 Keyboard input port on PolyMorphic Systems VTI board
FE00 Software write-protect port on IMSAI 4K RAM board

Using S-100 Video Display Boards

The video display boards for the S-100 bus are accessed thru both memory address locations and I/O ports. They are treated and used in the same manner as addition system RAM or I/O ports would normally be. The on board crystal option must be used with some video boards which normally derive their clock from bus line #49. Line 49 is a 2 MHz clock signal in 8080 systems, but is unused on the Kimsi board. Several video boards are also sensitive to the difference between the 6502 and 8080 SYNC signals. This is easily remedied as stated in the Application Notes for these boards.

Using PROM Programmers

There are several different types of PROM programmer boards which plug into the S-100 bus. In addition, there are several modules available which can be used with S-100 systems. These do not plug into the bus, but are out board (self contained) units which connect by cable to user provided I/O ports.

In the first category, boards which plug directly into the bus, there are some which program via memory addressing. These boards (such as The Prammer by XYBEK) require that the CPU stops (or waits) during a write instruction for programming to take place. Since the 6502 processor will not wait during a write cycle, these boards will not function properly in a Kimsi system (a compatible "Prammer" may be available in the future). Other plug in boards (such as THE PROM SETTER by Szerlip Enterprises) are addressed as I/O ports and should work well with Kimsi.

The second category, out board programming units, do not present any problems for the Kimsi system since they are used in conjunction with your existing I/O ports and do not connect directly to the S-100 bus.

Problems with S-100 Bus Boards

Here are a few tips for checking out S-100 bus boards.

If you cannot read/deposit data to a new RAM board, double check its address jumpers or switch settings; this is an easy place to make a mistake. Since empty, unused locations in the Kimsi system usually read "FF" on KIM's display, you may be able to tell that you're reading random data (e.g., data other than FF) from your RAM even though you can't deposit data to it. If this is true, your "read" circuitry is functioning but your "write" circuitry is faulty.

Remember that the instruction LDA F011 becomes A9 11 F0 in machine language.

Each board you add to your system draws additional power from your power supply. Be sure you have enough power available or erratic operation may result. Most S-100 boards must have an input voltage of approximately 7 volts; boards with battery backup circuitry need 7.5 or 8 volts.

Watch out for those heat sinks. They can and do run quite warm (hot). Try to avoid skin contact with them while you're poking around. This tip won't fix your system, but at least your system won't fix you.

Additional Hardware Information

Interrupts. The S-100 bus interrupt line (pin 73) is connected directly to IRQ on KIM. S-100 boards may interrupt KIM via this line as they would an 8080.

Since the S-100 bus doesn't usually have a NMI on it, the NMI line has been brought out to a normally unused pin, #17.

Reset. KIM may be reset from the S-100 bus by pulling the POWER-ON CLEAR (POC) line, pin 99, low.

DMA. Direct memory access may take place between boards on the S-100 Kimsi bus. A DMA request is made to the processor by a low signal on pin 72 (RDY) and a low signal on pin 74 (Processor Hold Request - PHOLD). When the CPU has stopped and the bus is available, pin 26 (Processor Hold Acknowledge - PHLDA) will go high. All address, data, and status lines will remain free for use until pin 72 or 74 returns high. Note: pin 24 ($\emptyset$ 2) does not tri-state; pin 26 PHLDA must be pulled up (1K to +5V) for proper operation.

Use of the reserved areas. It should be pointed out that much

of the reserved area is usable. If you've filled up the 52K area that is not reserved, or you just like to do things the hard way, the area from 0400-16FF and 1800-1FFF can be used for output only. You will not be able to read from this address range, but output boards used with memory addressing can be used there.

Adding custom boards to the S-100 bus. The following will give you an idea of the most simple way to add memory addressed devices to the S-100 bus. Each line coming in to the board typically draws 1 low power TTL load (in reality, Kimsi can handle 1 regular TTL load per line per slot). Output lines should be buffered for 1 regular TTL load and must be tri-state. Chip-select, board-enable signals should go TRUE when the address lines reflect the desired location. The input buffers (from D00-D07) may remain enabled at all times or enabled when the board is selected. The output buffers should be enabled when the board is selected AND pin 47 (SMEMR) is high. Writing or latching of data sent to the board should take place when the board is selected AND pin 68 (MWRITE) is high.

Empty connector pins. There are several pins on the Kimsi connector which are not used. Pin 5 connects to KIM's expansion pin 18 which is blank. This provides a handy way to get an additional signal from KIM to Kimsi (or vice versa) while still allowing easy connection and disconnection of the units. Non-KIM users should note that lines 6, 7, 18, 20, and C are also unused by Kimsi, and correspond to pins 17, 16, 5, 3, and X of a dual 22 pin connector at the CPU end of the cable.

S-100 Compatibility. In using an S-100 bus compatible system, several things should be remembered. First, the S-100 bus was designed around the 8080 CPU. Bus lines which reflect a signal unique to the 8080 processor (such as pin 28 which indicates the status of the internal interrupt enable flag) are difficult to simulate since there is no similar 6502/6800 signal. The lack of these signals rarely causes a problem. They are generally used only with boards which work specifically with the 8080 CPU.

Second, the S-100 bus is not yet a standard. Few manufacturers use all the defined pins on the bus and many differ in their use of each pin. With the many similar, unnecessary, and redundant pin functions on the S-100 bus, it is becoming more of a mess and less of a standard. If you have trouble using an S-100 board that is new to your system, take a minute to check the board's schematic. See which signals are used by the board and compare these pin numbers with the Kimsi "S-100 Bus Definition." If the Kimsi use (noted in parenthesis) of any pin differs from the standard S-100 bus usage, modification of the S-100 board may be necessary. For example, a board which connects to pin 25 (Ø1) would need modification, since pin 25 is "not used" on the Kimsi board. Forethought Products will supply modifica-

tion information and make an application note available on S-100 boards which are found to be not plug-in compatible with Kimsi. If you suspect a board to be incompatible with Kimsi, send us the schematic and operating information for the board and it will receive our immediate attention.

Third, the cycle times for 8080 CPUs are longer than those of a 6502. Because the 6502 cycle times are shorter, there is less tolerance to delays within the system. An extra gate or buffer which a manufacturer put onto their board may have no effect on the relatively "loose" 8080 timing, but might pose a problem in getting the signal to the 6502 CPU in time for processing. It's possible then to have a board which is electrically and logically compatible with the S-100 bus but will not operate correctly with Kimsi (without slowing KIM down slightly- about a 1% speed reduction).

The best "weapon" against bugs is to stick with boards that are known to be Kimsi compatible and to make such information available to all Kimsi users. If you have an S-100 bus board that you're happy with, drop us a note so that it can be added to the list. If you've found a problem with a board, send us a schematic and tell us about the problem. If your letter requires a reply, please include a return envelope.

S-100 bus definition. The following definition is given for the standard S-100 bus. Differences or comments about the Kimsi/S-100 bus are shown in parentheses.

S-100 BUS DEFINITION

All signals are TTL. Address and data lines are TRUE logic (1=+5V). "P" prefix indicates a processor command or control signal; "S" prefix indicates a processor status signal.

PIN	SYMBOL	USE
1	+8V	+8 volts - Input to 5V regulators.
2	+16V	+16 volts - Source of positive unregulated voltage.
x 3	XRDY	External Ready (Not used).
x 4	V10	Vectored Interrupt Line 0
x 5	V11	
x 6	V12	
x 7	V13	
x 8	V14	
x 9	V15	
x 10	V16	
x 11	V17	
12-16	UNUSED	
17	(<u>NMI</u>)	Normally unused (<u>NMI</u> from 6502).
x 18	<u>STATUS</u> <u>DSBL</u>	Tri-states the 8 status lines (Not used).
x 19	<u>CC</u> <u>DSBL</u>	Tri-states the 6 command/control lines (Not used).
20	UNPROT	Unprotects currently addressed memory board (Tied low).
x 21	SS	Single step control (Not used).
x 22	<u>ADDR</u> <u>DSBL</u>	Tri-states the address lines (Not used).
x 23	<u>DO</u> <u>DSBL</u>	Tri-states the data lines (not used).
* 24	ø2	Phase 2 clock (Does not tri-state when the processor HOLDS).
25	ø1	Phase 1 clock
26	PHLDA	Hold Acknowledge (Address, data, status and cc lines are tri-stated when PHLDA=1).
27	PWAIT	Acknowledges that processor is waiting (See PIN 72).
x 28	PINTE	Indicates interrupt enabled (Not used).

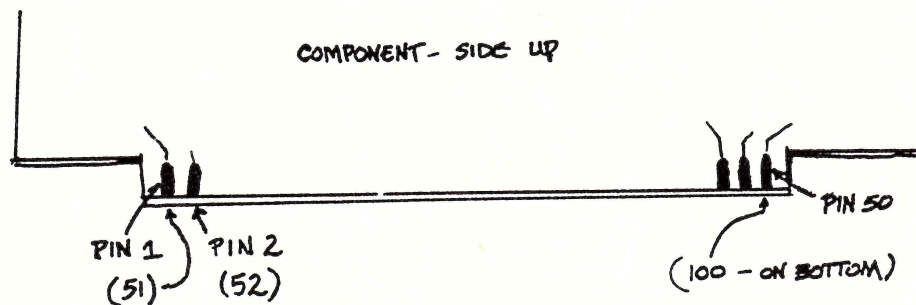
29	A5	Address line 5
30	A4	
31	A3	
32	A15	
33	A12	
34	A9	
35	D01	Data Out line 1
36	D00	
37	A10	
38	D04	
39	D05	
40	D06	
41	DI2	Data In line 2
42	DI3	
43	DI7	
* 44	SM1	Indicates a processor fetch cycle (Indicates the beginning of each instruction cycle).
45	SOUT	Indicates that address bus contains address of an output device, data bus is stable when $\overline{PWR}$.
46	SINP	Indicates address bus contains address of input device, data should be placed on bus when $\overline{PDBIN}$.
47	SMEMR	Current cycle will be a memory read.
✗ 48	SHLTA	Acknowledges a HALT instruction (Not used).
✗ 49	$\overline{CLOCK}$	2 MHz clock signal (Not used).
50	GND	Ground
51	+8V	
52	-16V	Source of negative unregulated voltage.
✗ 53	$\overline{SSW DSB}$	Sense switch disable (Not used).
✗ 54	$\overline{EXT CLR}$	External Clear (Not used).
55-60	NOT USED	
61	(KRDY)	(Used when KIM is sharing the S-100 bus with another CPU).
62	(KØ2)	(Used with additional CPU).
63	($\overline{KHOLD}$)	(Used with additional CPU).

64-66 NOT USED

x	67	<u>PHANTOM</u>	Used by Processor Technology during system start-up (Not used).
	68	MWRITE	Data on the Data Out bus is to be written into the currently addressed memory location.
x	69	<u>PS</u>	Used to indicate the status of protected memory boards (Not used).
x	70	PROT	Protects currently addressed memory board (Tied low).
x	71	RUN	STOP/RUN signal from front panel (Not used).
	72	PRDY	Pull low to freeze processor at current address (can be used on read cycles only).
	73	<u>PINT</u>	Interrupt Request - Request is not honored if the processor is in a HOLD state or if the interrupt disable flag is set.
	74	<u>PHOLD</u>	Processor HOLD request (processor tri-states all bus lines when the request is acknowledged - see PIN 26).
	75	<u>PRESET</u>	P. Reset - Program counter is cleared and instruction register is set to 0 (Not used).
✓	76	PSYNC	Indicates the beginning of each machine cycle
✓	77	<u>PWR</u>	P. WRITE - Data on the Data Out bus is stable when <u>PWR</u> .
✓	78	PDBIN	P. DATA BUS IN - Data should be placed on the Data In bus when PDBIN.
	79	A0	Address line 0
	80	A1	
	81	A2	
	82	A6	
	83	A7	
	84	A8	Data Out line 2
	85	A13	
	86	A14	
	87	A11	
	88	DO2	
	89	DO3	Data In line 4
	90	DO7	
	91	DI4	

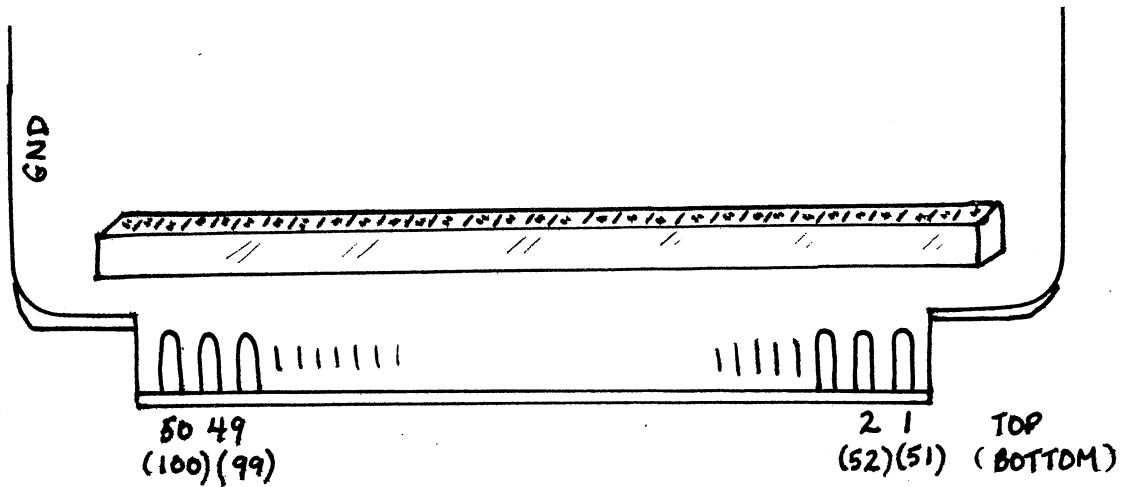
✓	92	DI5	
	93	DI6	
	94	DI1	
	95	DI0	
✓	✗ 96	SINTA	Interrupt Acknowledge (Not used).
✓	97	SWO	Current machine cycle will be a write memory or output function (same as $\overline{R/W}$ from 6502).
✓	✗ 98	SSTACK	Indicates that the address bus holds the pushdown stack address from the Stack Pointer (Not used).
✓	99	$\overline{POC}$	Power-On Clear (Resets the 6502).
✓	100	GND	Ground.

S-100 BUS PLUG-IN CARD



PIN LOCATIONS: { 1-50 on top
51-100 down under

BUSTAP. The BUSTAP provides a convenient way to attach to the system bus for experimenting, trouble-shooting, and expanding the system. The pin identification diagram is shown below.



BUSTAP PINOUT

KIMSI PINOUT

PIN #	FUNCTION	PIN #	FUNCTION
1	GND	A	RAM/R/W
2	+5V (out)	B	$\overline{\text{O2}}$
3	+12V (out)	C	
4	$\overline{\text{K-ENABLE}}$	D	$\overline{\text{R/W}}$
5		E	R/W
6		F	O2
7		H	AB15
8	DB0	J	AB14
9	DB1	K	AB13
10	DB2	L	AB12
11	DB3	M	AB11
12	DB4	N	AB10
13	DB5	P	AB9
14	DB6	R	AB8
15	DB7	S	AB7
16	RST	T	AB6
17	$\overline{\text{NMI}}$	U	AB5
18		V	AB4
19	$\overline{\text{IRQ}}$	W	AB3
20		X	AB2
21	RDY	Y	AB1
22	SYNC	Z	AB0

NOTE

Pin 4 is low when the address lines equal 0000-1FFF or FYXX (where Y = 1, 3, 5, 7, 9, B, D, F, and X = any digit).

WARRANTY

Kits. All parts and materials are warranted for a period of 90 days. A replacement part will be sent when the defective part is returned to the factory along with a note of suspected malfunction and the serial number of the unit.

Factory Assembled Units are warranted for 120 days following purchase. Defective units which are sent to the factory post-paid will be repaired and returned at no charge.

This warranty is void for parts that, in the opinion of Forethought Products, have been damaged thru misuse by the purchaser, and is limited to repair or replacement of the Forethought Products unit which is defective.

Send defective units to:

Forethought Products
P.O. Box 8066
Coburg, OR 97401

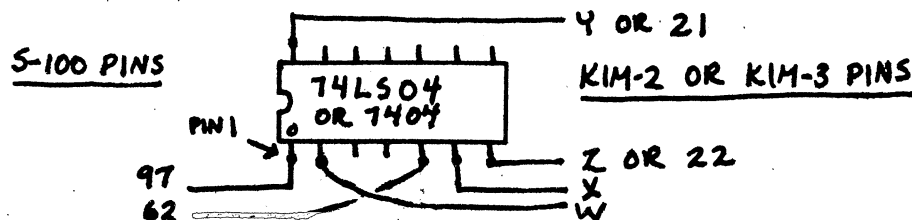
PRELIMINARY

Using KIM-2 or KIM-3 with Kimsi

The KIM-2 or KIM-3 may be connected to Kimsi via the BUSTAP connector as shown below.

BUSTAP	KIM-2 or KIM-3 CONNECTOR	USE
50, 100	A, Z, 1, 22	GND
79	B	AB0
80	C	AB1
81	D	AB2
31	E	AB3
30	F	AB4
29	H	AB5
82	J	AB6
83	K	AB7
84	L	AB8
34	M	AB9
37	N	AB10
87	P	AB11
33	R	AB12
85	S	AB13
86	T	AB14
32	U	AB15
43, 90	8	DB7
40, 93	9	DB6
39, 92	10	DB5
38, 91	11	DB4
42, 89	12	DB3
41, 88	12	DB2
35, 94	14	DB1
36, 95	15	DB0
1, 51	19, 20	+8

In addition, the following modifications must be made. Cut the foil trace between U13 pin 2 and U12 pin 1 and 2. Connect a wire from KIM-2(3) pin W to U12 pins 1 and 2. Cut the foil trace between U13 pin 4 and U5 pin 13. Connect a wire from KIM-2(3) pin X to U5 pin 13. If you do not want to modify the board you may use the following circuit instead.



The KIM-2 or KIM-3 boards(s) may be located at any address between 2000-EFFF that is not being used by other memory boards in the system.

PRELIMINARY

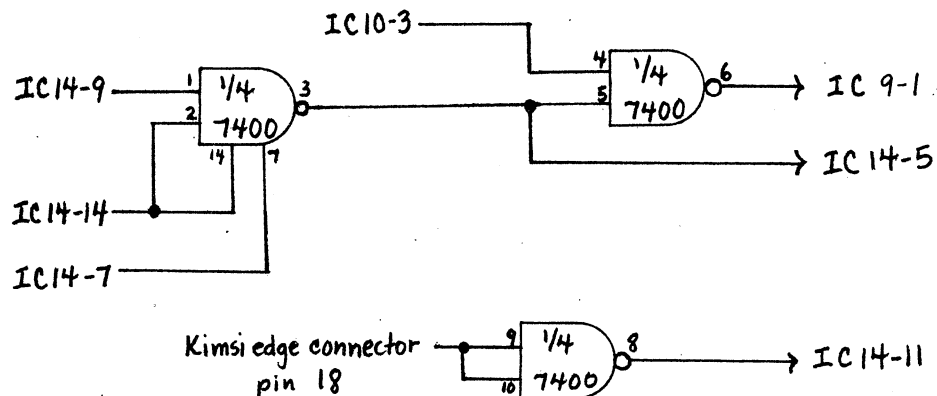
Using KIM-4 with Kimsi

Because production of KIM-2, KIM-3, and KIM-4 has been virtually discontinued, we would suggest that the KIM-4 motherboard not be used unless you already have several KIM-2/3 boards on hand. Without meaning to offend KIM-4 users, it appears to be a better use of time and energy to connect a KIM-2/3 directly to Kimsi, or even remove the memory chips for use on S-100 boards (bare memory boards are \$20-\$30) than to bother with the KIM-4 connection with Kimsi.

Connection of Kimsi to the KIM-4 expansion connector is made thru two dual 22-pin connectors. For reference, label the "Top" of each, and one as "KIM-4" and the other as "Kimsi." Then, using short (4-5") wires, wire the connector as shown below.

Kimsi Pin#	KIM-4 Pin#	NAME	Kimsi Pin#	KIM-4 Pin#	Name
Z	B	AB0	8	15	DB0
Y	C	AB1	9	14	DB1
X	D	AB2	10	13	DB2
W	E	AB3	11	12	DB3
V	F	AB4	12	11	DB4
U	H	AB5	13	10	DB5
T	J	AB6	14	9	DB6
S	K	AB7	15	8	DB7
R	L	AB8	17	6	NMI
P	M	AB9	16	7	RST
N	N	AB10	19	4	TRQ
M	P	AB11	B	V	$\emptyset 2$
L	R	AB12	F	X	$\emptyset 2$
K	S	AB13	E	W	R/W
J	T	AB14	1	Z	GND
H	U	AB15	22	2	SYNC
18	16	BD SEL			

The following circuit involves one IC and can be constructed in the Kimsi prototype area. Connections to existing Kimsi ICs are made with a wiring pencil or small wires.



Disable the decoding circuitry on Kimsi by cutting the trace on the back of the board between IC11 and IC13. It is a "V" shape for easy identification. Cut out part of this "V" (the decoding circuitry can alternately be disabled by removing IC11, bending pin 11 outward, and reinserting IC11).

Connect power supply leads (+8, +16, and GND) to both KIM-4 and Kimsi. Both motherboards can now be used in their normal manner.

NOTE: The "proper" way to connect KIM-4 and Kimsi to KIM is to wire both boards to KIM's expansion connector. This is all but impossible due to the combination of edge connectors that these boards use. The interconnection scheme used here is logically sound, but may have problems due to delays incurred when signals must travel thru both the Kimsi and KIM-4 buffers before they can reach KIM. The ultimate cure for this problem would be to slow KIM's clock slightly.

Using Kimsi with Non-KIM Systems

This note does not refer to any other particular system, but 6502/6800 systems in general. In the future, specific application notes may be written for systems which are found to have unusual connection problems. In addition, plug-compatible adaptor boards will be available (from Forethought Products) for several popular 6502/6800 systems in the near future.

To connect a system to Kimsi is relatively simple since there is very little additional circuitry needed. The Kimsi prototype area can usually accommodate any extra interface chips that are required.

The first step of interconnection is to bring each address and data line to the proper pin on a 44 pin connector (which will attach to Kimsi). Keep your CPU board as close as possible to Kimsi; cables longer than six or eight inches can cause some trouble. The address and data lines do not need to be buffered; they may come directly from the CPU chip. Use the "Kimsi Pinout" listing to connect each line to the proper connector pin (dual 22 pin connectors have the pin numbers stamped near each pin). Also connect the RST, NMI, IRQ, RDY, SYNC, and GND (ground) to the proper pins.

Kimsi provides 1 amp of 5 volt regulated power for your CPU board. Connect to pin 2 for this 5 volt power, otherwise leave this pin unconnected. If your CPU board has its own regulator, a source of unregulated voltage is available by connecting to pin 5. To use this option, the pad from pin 5 on Kimsi must be jumpered to the "+" lead of C2. Pin 3 is a source of +12 volts. This pin should only be used however, if your CPU board draws less than 60 ma of 12 volt power.

Pins A, B, D, E, and F are control signals. These signals must be buffered and should not be taken directly from the CPU. Many systems with on-board RAM have the RAM/R/W signal needed at pin A. You may tap this line on your board, or duplicated it as shown in Fig. A. This circuit is easily built in the Kimsi prototyping area. Use a wiring pencil or small wires to connect to the Kimsi IC pins as shown in parenthesis. Fig. A assumes that the R/W has been connected to pin D. If your CPU board does not have the R/W signal available, the circuit in Fig. B should be used. Fig. B also supplies $\overline{Q2}$, which is not available in some systems.

The only remaining signal needed by Kimsi is pin 4, K-ENABLE. The K-ENABLE signal is used to tell Kimsi when to "turn off." This prevents Kimsi from sending data to the CPU chip when the CPU is "talking" to a device on its own board. Kimsi normally

reserves 0XXX, 1XXX, and FXXX for use by the CPU. This leaves 2000-EFFF for use by boards which plug into Kimsi. If your CPU board devices (RAM, ROM, I/O, etc.) can be located in the normally reserved areas (0XXX, 1XXX, FXXX), then no connection to pin 4 is necessary. If on-board devices are used in other areas of memory, the circuitry in Fig. C should be used. In this circuit, the CS (chip select) signal from each on-board device is connected to an input of the 7430 (eg. a CPU board with one ROM and one I/O chip would make a connection from the ROM $\overline{CE}$ pin and the I/O chip $\overline{CE}$ pin, to pins 1 and 2 of the 7430). These extra signals can be brought to Kimsi via pins 5, 6, 7, 18, 20, or C. The corresponding pads for these pins are then jumpered to the prototype area (7430-1, 2, 3, etc.). To use the Fig. C circuitry the normal decoding circuitry on Kimsi must be disconnected. This is accomplished by cutting a foil trace which runs on the bottom of the board. It is located between IC11 and IC13, and forms a "V" shape for easy identification. Cutting out part of the "V" disconnects the normal K-ENABLE decoding circuitry.

Questions concerning connection of "other" CPU boards to Kimsi should include a schematic of the CPU board and a listing of the address areas which are located on the CPU board (ie, a system map). A return envelope will help to speed our reply.

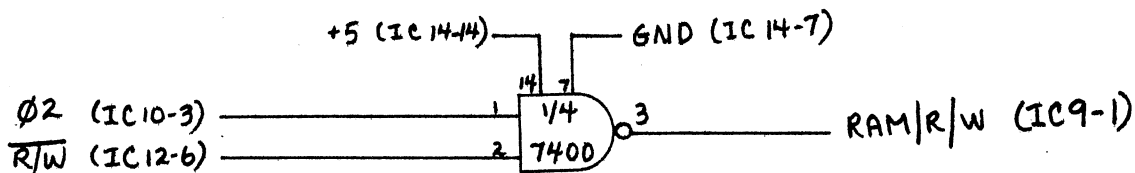
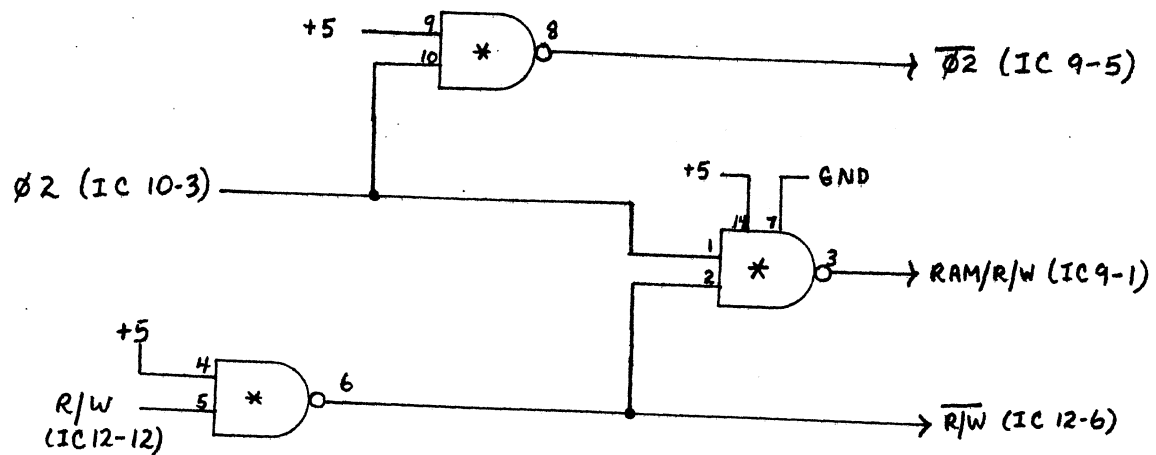


Fig. A



* = $\frac{1}{4}$ 7400

Fig. B

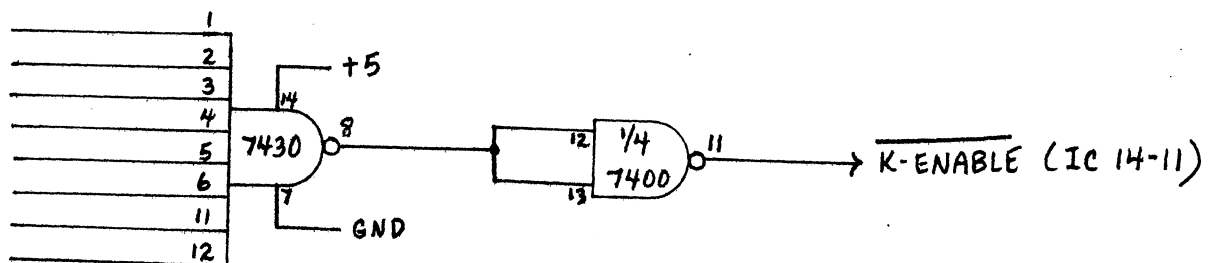


Fig. C

Using Ribbon Cables between KIM and Kimsi

There are some situations where it is desirable to connect KIM and Kimsi by ribbon cable rather than a rigid connector. Although this is possible, and works well in some situations, there are other situations where it is not advised.

It should be kept in mind that the KIM board was designed for direct connection to a motherboard as there is no on-board buffering of address or data lines. The other problems which arise are cable crosstalk and propagation delay. It's often an easy matter to construct a cable and find it 100% reliable for your present system. The catch is the "present" system. Your cable may become unreliable as system (hardware) changes are made.

We ran a Kimsi system connected by a single ribbon cable (data and address lines alternating in the cable) for several weeks. It was tested and proven to be reliable. The problem occurred when we changed the jumpers on one of the memory boards so that it would reside at a new address. Now we found that the same cable was unable to successfully run a memory test. Moving the memory board had set up a different crosstalk pattern on the cable and was interfering with data transmission.

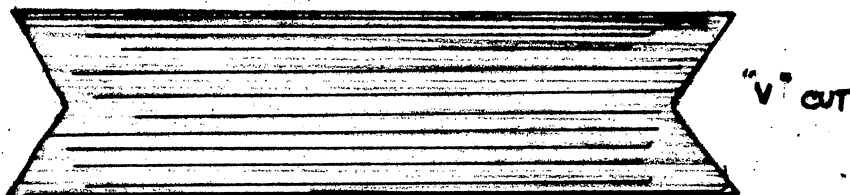
Separating the cable into two 22 line ribbons (one for data, one for address) helped the crosstalk problem, but after running this "100% reliable" cable for awhile, we found an S-100 board (which we were testing for the first time) that had three or four memory cells that wouldn't pass the memory check. After swapping memory chips there were still problems in reading memory correctly. Replacing the ribbon cable assembly with a rigid connector cleared up the problem. Why? This particular board had been designed with several more gates than usual along the signal path. These gates delayed the signals enough that they were barely able to reach the CPU in time for proper processing. The extra propagation delay caused by the cable slowed these signals beyond the point of reliability. Propagation delay problems are a function of buffering stages on the S-100 board, cable delay, timing tolerance of KIM's CPU, and deviation of KIM's crystal. Although we have not yet run any tests, propagation delay problems (for cables several feet long) should disappear if KIM's clock frequency is lowered from 1MHz to 980 KHz or so.

We conclude that ribbon cable assemblies can be used with success, but that they necessitate thorough system checking when hardware changes are made. As their performance can vary depending on system configuration, they must as a whole be considered unreliable.

Constructing a Ribbon Cable Connector Assembly

The following cable construction has been successful in lengths up to two feet. However propagation delays in unmodified systems (1MHz clock) usually holds the length to eight or ten inches.

Prepare two lengths of 22 conductor ribbons cable by cutting each end in a "V" as shown below.



Separate the wires in the cable by making a 2" slit between each conductor with regular household scissors (the scissors won't be harmed as you're cutting insulation, not wire). Strip $\frac{1}{4}$ " or so of insulation from each wire. Place the ribbon in a vise (or other holder) and tin (apply solder to) each bare wire end.

Place the dual 22 pin connector in a holder, and tin each of the 44 pins. Hold the ribbon cable near the connector and position the outside wire on terminal 22. Hold the wire in place and apply heat to the joint. Since both surfaces have been tinned, they will melt together without additional solder (convenient for those of us with only two hands). Place the next wire in the ribbon on pin 21 and heat. Repeat for the 20 remaining wires. Turn the connector over and attach the other length of cable to pins A-Z. Tin the pins on the other dual 22 pin connector and place it in a holder with pin 22 up. Find the wire which is connected to pin 1 on the completed connector. Connect this wire to pin 22 on the uncompleted connector. Solder (heat) the next wire to pin 21, etc. Turn the connector over, and attach the wire from pin Z to pin A, etc.

Place a "TOP" label on the numerical (1-22) side of both connectors (attaching a connector upside down can damage KIM). Check that the cable is connected as follows:

PIN	to	PIN
1	-	22
2	-	21
3	-	20
'	-	'
'	-	'
20	-	3
21	-	2
22	-	1

PIN	to	PIN
A	-	Z
B	-	Y
C	-	X
'	-	'
'	-	'
X	-	C
Y	-	B
Z	-	A

Connect applications pins K and N (See "Connecting KIM to Kimsi), be certain both connectors are "TOP" up, and apply power to Kimsi. If the display doesn't light, remove power and recheck connections. When the display is operational, load the following program.

Memory/Cable Test Program (starting at 000A hex)

```
(000A) A000 A504 8500 A505 8501 A9FF 8502 E602 A502 9100 B100
C502 F00B 8503 A9FF 85FA 85FB 4C161C A502 D0E5 E600 A500 D002
E601 A501 C507 D0D7 A500 C506 D0D1 A900 85FA 85FB 4C161C
```

Test each memory board in your system by inserting its starting address in location 0004 (low) and 0005 (high). Ending address +1 goes in 0006(low) and 0007 (high). Start the program at 000A. It will write and read the 256-bit patterns in each cell in the test range. It will display 0000 upon completion. Errors cause a display of FFFF. Pressing the "+" button will display the faulty address (low) at 0000 and 0001 (high). The data written appears in 0002 and the bad data read is at 0003. If there are no errors, modify 004E to 0A and 004F to 00. This will repeat the test indefinitely. Running it for an hour without an "FFFF" display insures absolute reliability. Note: This program takes approximately 9 seconds per 1K memory. If any of your boards don't pass the test try the following:

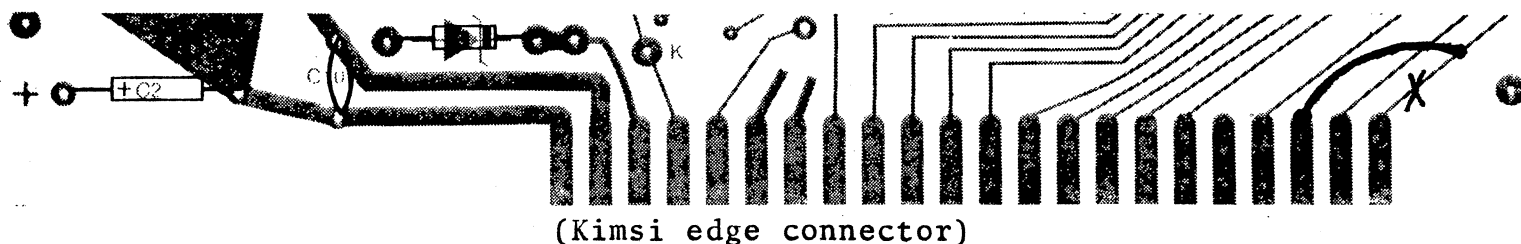
1. Add an extra ground wire (KIM pin 22, Kimsi pin 1) between the connectors.
2. If all the bad data words have bits low which were written high, add eight 1K (or less) resistors at the KIM connector. Solder one resistor each to pins 8, 9, 10, 11, 12, 13, 14, and 15. Solder the other end of all eight resistors to pin 22 (GND).
3. Shorten the length of the cable or slow KIM's clock by replacing the crystal or using an RC Network (MOS Technology Technology Hardware Manual page 43).

Kimsi Application Note #A6

Using the PolyMorphic Systems Video Terminal Interface (VTI)

The PSYNC requirements of the VTI board are quite different from most S-100 boards. The easiest way to remedy this situation is to modify Kimsi as shown below. This modification will not be necessary on future versions of Kimsi as it will be incorporated into a permanent change of Kimsi's circuit pattern.

- Cut the circuit trace at the 'X', and install a short jumper as shown.



Since a 2MHz clock signal is not present on the Kimsi bus, the VTI board must have its on-board crystal option implemented when it is used in a Kimsi system. The following are the specific steps necessary to install this option:

- Set Jumper 1 for 'non-Poly' system (see page 17 of the manual).
- Set Jumper 5 for on-board crystal (cut existing jumper trace).
- Install a 2MHz crystal and 10pf capacitor in the space provided on the board.
- Use a small wire to connect IC29 pin 8 to IC29 pin 11. This connection is missing from the board's circuit pattern.

The following modification should be made only if the VTI's keyboard input port will be used.

- Connect IC6 pin 12 to IC8 pin 14.

Set all address switches to 'off' and install the board into Kimsi. The video RAM should now be accessible at EC00-EFFF (64 character option). The keyboard input port can be read at FC00. Reading FC01 gives you the keyboard interrupt signal on DB0 (=0 when there is data latched into the keyboard port) and the actual keyboard **strobe** on DB7. The following subroutine can be used to read a character from the keyboard: AD01FC 2901 D0F9 A900FC 60.

The VTI remains IMSAI/Altair system-compatible when this modification has been made. The RAM and keyboard address will remain as above (EC00-EFFF and FC00).

All IC and pin numbers are per VTI board Rev. 1.2.

Kimsi Application Note #A7

Using the Godbout 4K RAM Board

The Godbout 4K Econoram board schematic shows IC41 pin 1 connected to ground. In reality, this pin is not ground, but connects to S-100 pin 96 (SINTA - Interrupt Acknowledge). SINTA is normally at ground on 8080 systems, but is open (no connection) on the Kimsi board. The problem is remedied by shorting the Econoram IC41 pin 1 to the ground foil which runs directly above it on the back of the board OR by using a short wire to connect S-100 pin 96 to S-100 pin 100 (GND) on the bottom of the Kimsi board. Note: this problem does not exist on the 8K Econoram board.

PRELIMINARY

Kimsi Application Note #A8

Using the Processor Tech. Video Display Module (VDM-1) Board

Due to the PSYNC requirements of this board, make the following change to the VDM-1 when using it with Kimsi (applies to VDM-1 board revisions C, D? and E):

Remove IC18 from its socket, bend pin 5 outward, and replace the IC in its socket.

Kimsi Application Note #A9

Using the Vector Graphics PROM/RAM Board

When using this board with Kimsi, the jumper options should be set as follows: 6-7 open (cut trace); 8-9 open (cut trace); 10-11 open.

Although the RAM section of this board will operate correctly with Kimsi, the following modifications are necessary to implement wait states for slow PROM's (applies to PROM/RAM board revision 3).

- Remove IC C3 from its socket, bend pin 4 outward, replace the IC in its socket.
 - Solder a short jumper between pins 2 and 4 on IC C3.
 - Solder a jumper from IC C6 pin 9 to IC C3 pin 3.
 - Modify the Kimsi board as shown in App. Note A6.
-

Kimsi Application Note #A10

Using the Solid State Music VB1B Video Board

To use the VB1B with Kimsi, make the following modification:

Remove U17 from its socket, bend pins 4 and 5 outward, and replace the IC in its socket.

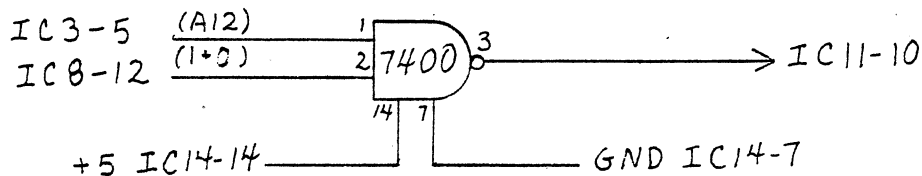
It may be desirable in some applications to use address space on Kimsi which is not normally available to S-100 boards. The following modifications allow for S-100 use in two of these areas.

Kimsi Application Note #A11

Using Block 0000-0FFF on Kimsi

This modification allows a 4K S-100 memory board to be used between address 0000-0FFF (an area normally reserved for KIM). Because S-100 boards are decoded only in 4K blocks, this modification removes KIM's on-board 1K memory from use.

1. Cut the trace between IC9 Pin 4 and IC11 pin 10 (see "A" on the attached schematic).
2. Implement the following circuit in the Kimsi prototype area:



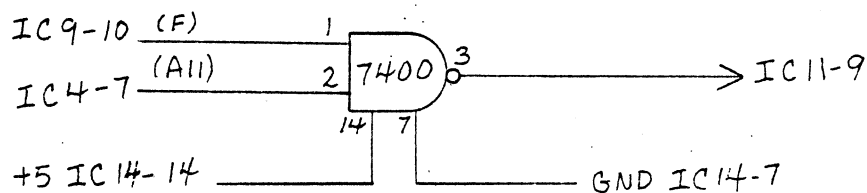
Note: IC11-10 means IC11 pin 10

Kimsi Application Note #A12

Extending the S-100 Memory Area to F800

To extend the S-100 memory area from F000 thru F7FF:

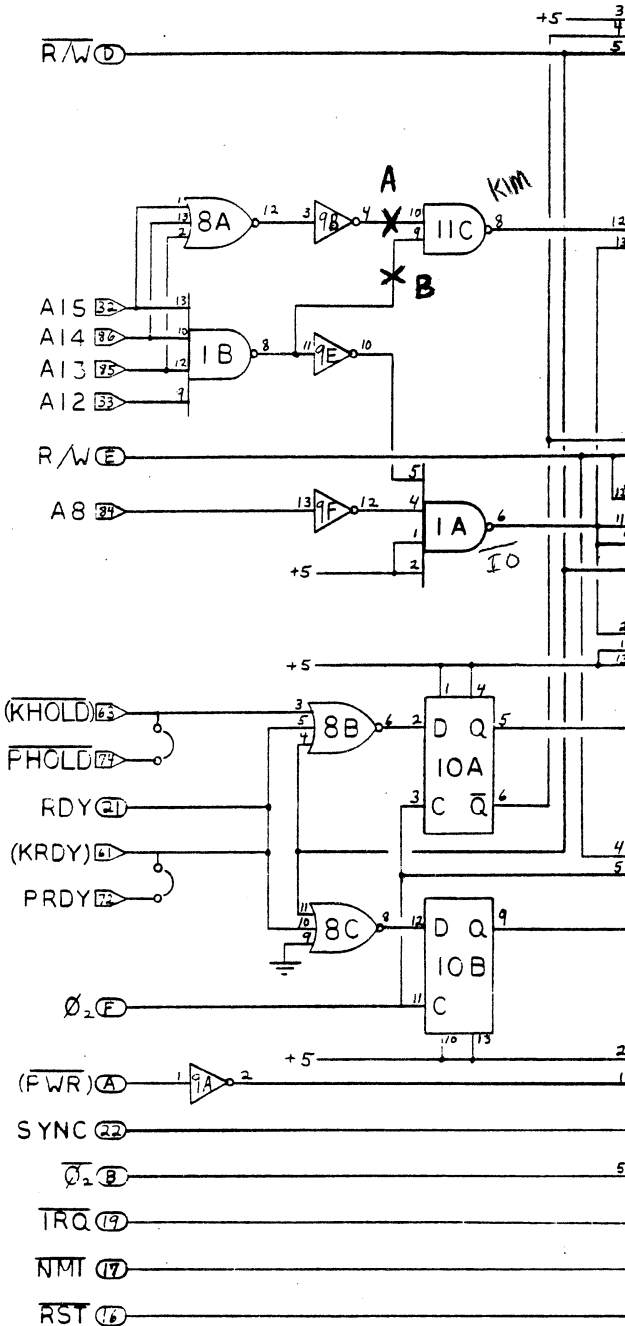
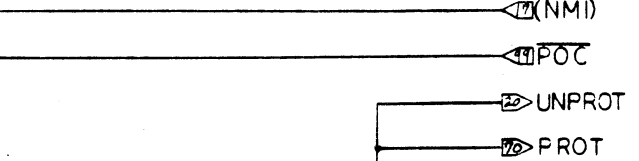
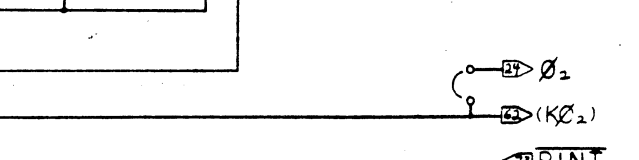
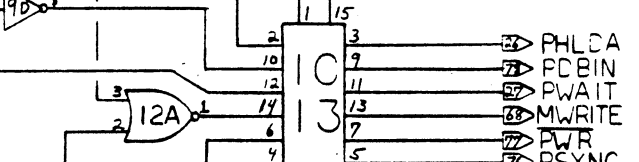
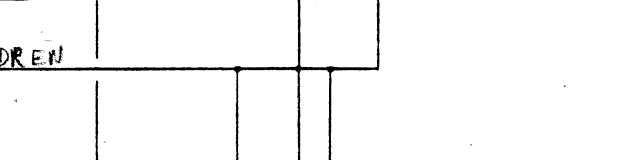
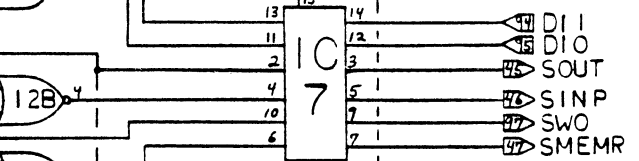
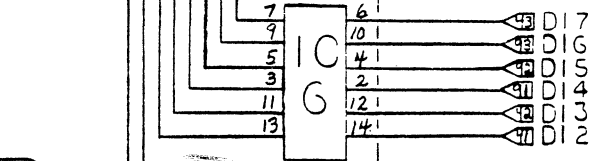
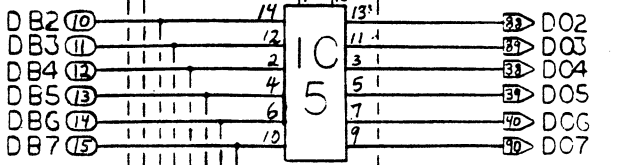
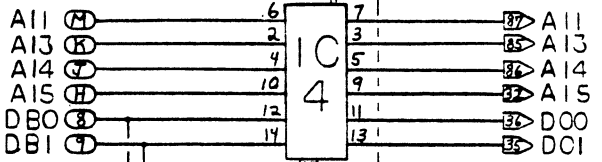
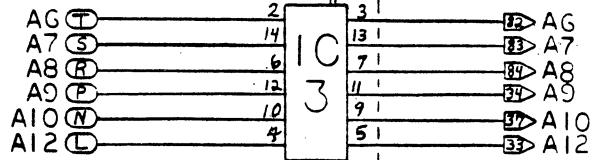
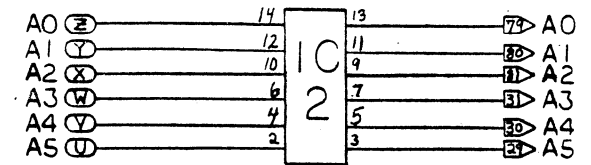
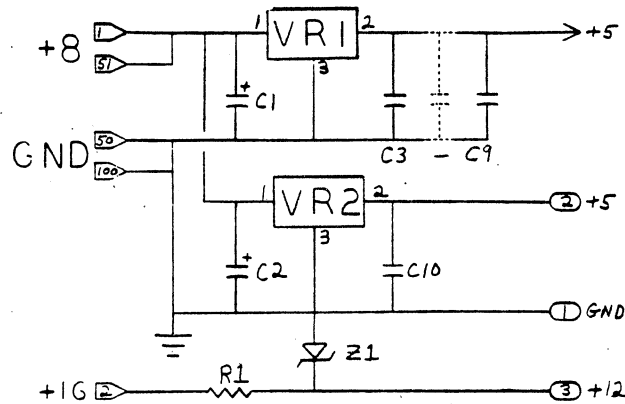
1. Cut the trace between IC1 pin 8 and IC11 pin 9 (see "B" on attached schematic).
2. Implement the following circuit in the Kimsi prototype area:



Note: IC11-14 means IC11 pin 14

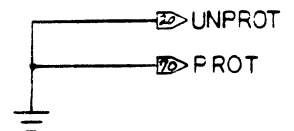
S-100 memory may now be used on Kimsi from 2000 thru F7FF.

KIM/S-100 Bus Interface
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Connector Symbols

- Kimsi edge connector finger
- Connection to S-100 bus



PRELIMINARY

Kimsi Application Note #A14

Using DC Hayes 80-103A Modem Board

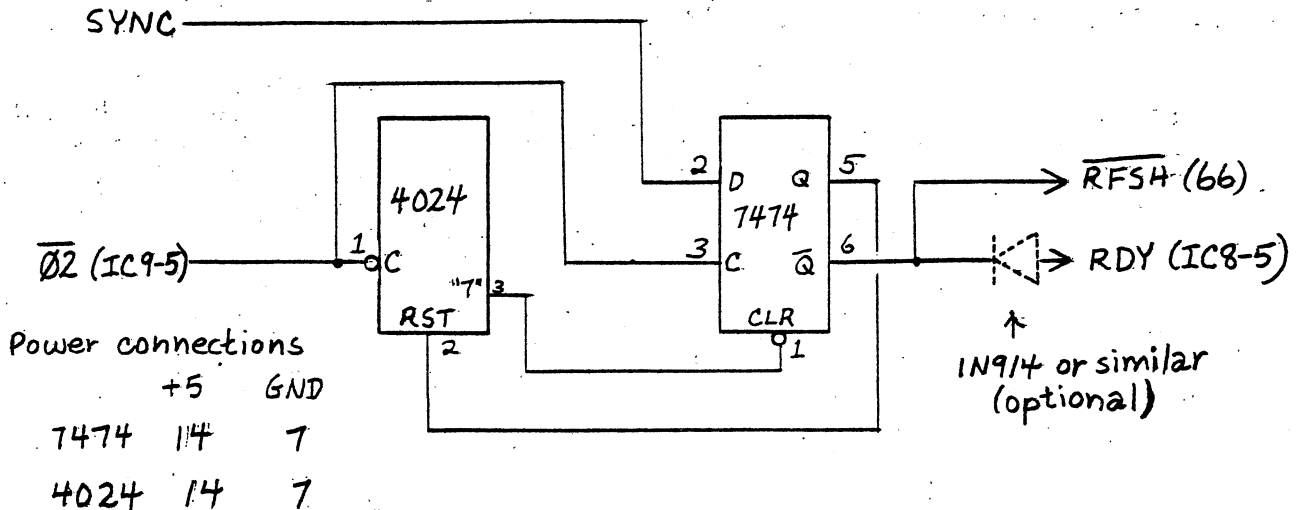
Because the 80-103A uses the upper address lines for its I/O "port number" it is probably best to use this board at a memory location (see 80-103A Manual page 3.8).

To prevent unintentional resetting of the 80-103A, make the following modification to the board: remove U24, bend pin 12 outward, and reinsert the IC.

Kimsi Application Note #A15

Using the SD Sales "Expandoram" Dynamic RAM board

The SD Sales Expandoram Dynamic memory board can be used with Kimsi by adding the following refresh circuit to the Kimsi prototype area.



Note: The SYNC signal should be taken from the edge connector finger nearest the prototype area on the topside of Kimsi (Kimsi pin #22). The -RFSH line is connected to S-100 pin #66.

The optional diode is required only when other cards affecting the RDY lines are present in the system. It is normally not needed.

In addition to the circuit shown above, the Expandoram board itself must be modified slightly as detailed in the attached Application Note #B1.

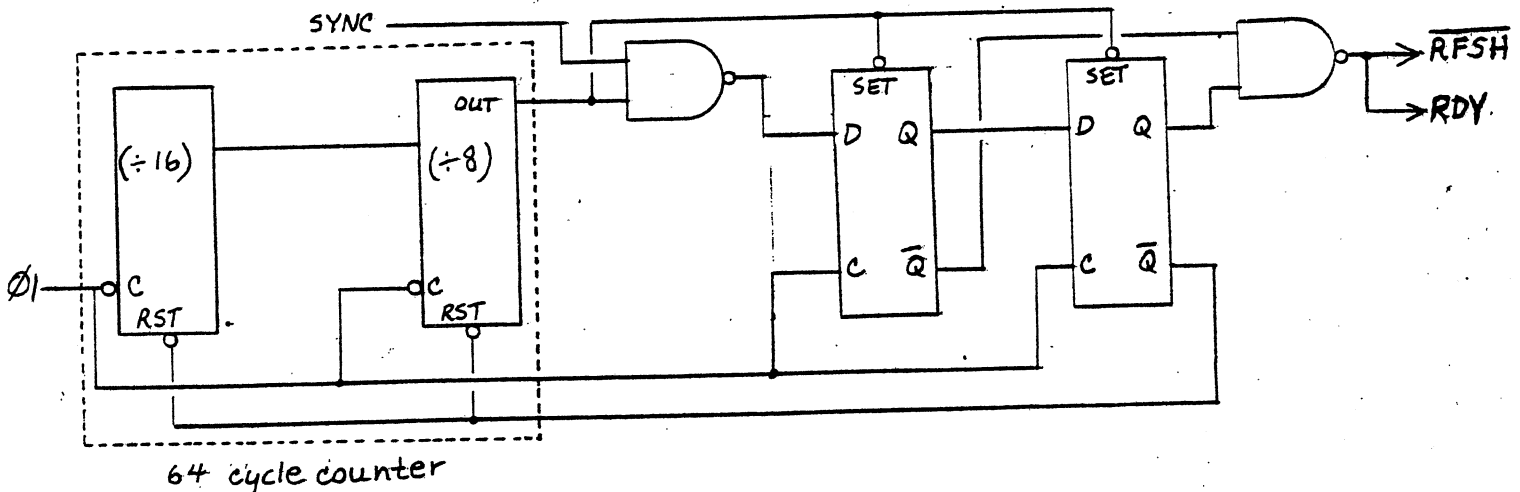
Testing Dynamic RAM

In running functional tests on dynamic RAM boards, keep in mind that normal memory tests will detect bad cells, address decoding errors, etc., but they will in no way test the refresh circuitry associated with the RAM. Because it can often take $\frac{1}{4}$ second or more for a cell (that is not being properly refreshed) to lose its charge, and because the act of reading or writing a dynamic memory cell causes that cell (and other related cells) to be refreshed, the dynamic memory test program should write a byte or pattern of bytes to the RAM board and then wait for a length of time. By entering a delay loop and waiting $\frac{1}{4}$ second or so before checking the data that was written, cells which are not being properly refreshed will have time to lose their charge and can be detected during the checking phase of the test.

Refresh Circuit Notes

Although it may not be the best designed card around, the Expandoram board is one of the few dynamic RAM cards that allows external (off-card) control of the refresh cycles. Because the system can control the refresh timing, we can guarantee that the CPU will not try to access a board that is trying to refresh itself (a fatal condition for a 6502 in a write cycle). This is unavoidable with most dynamic RAM boards that refresh themselves and expect the CPU to wait if they're busy.

The refresh circuit design in the Kimsi Application Note is a straight-forward circuit derived from the logic shown in the MOS Tech. 6502 Hardware Manual, page 116. Since the Expandoram board requires a minimum of one refresh period every 64 us, the circuit could be easily completed as shown below.



Refresh for 1 cycle every 64us = $1/65 = 1.5\%$ time refreshing
(98.5% time processing)

After the counter determines that a refresh period is needed, the circuit waits for a SYNC at the beginning of ϕ_1 (end of the last machine cycle). Since a write cycle will never follow a SYNC cycle, it proceeds to pull the RDY line low (stopping the CPU) and signals the RAM board to execute one refresh cycle. The circuit holds the RDY line low for exactly one clock cycle and releases it on the following ϕ_1 clock pulse. The circuit shown in Kimsi App. Note #15 is a refinement of this circuit which has exactly the same function and timing as the one shown above.

The modifications to the Expandoram board itself are necessary to make it more compatible with the 6502 cycle (or the Z-80 for that matter). Although you may note that pin 75 (-RESET) on the Kimsi is "floating", the Expandoram's -RESET line will not be affected by noise, etc. This is because the line must be held low for at least four cycles before any action takes place on the card (and noise will never last that long).

Betsi Application Note #B1

Using the SD Sales EXPANDORAM board with Betsi or Kimsi

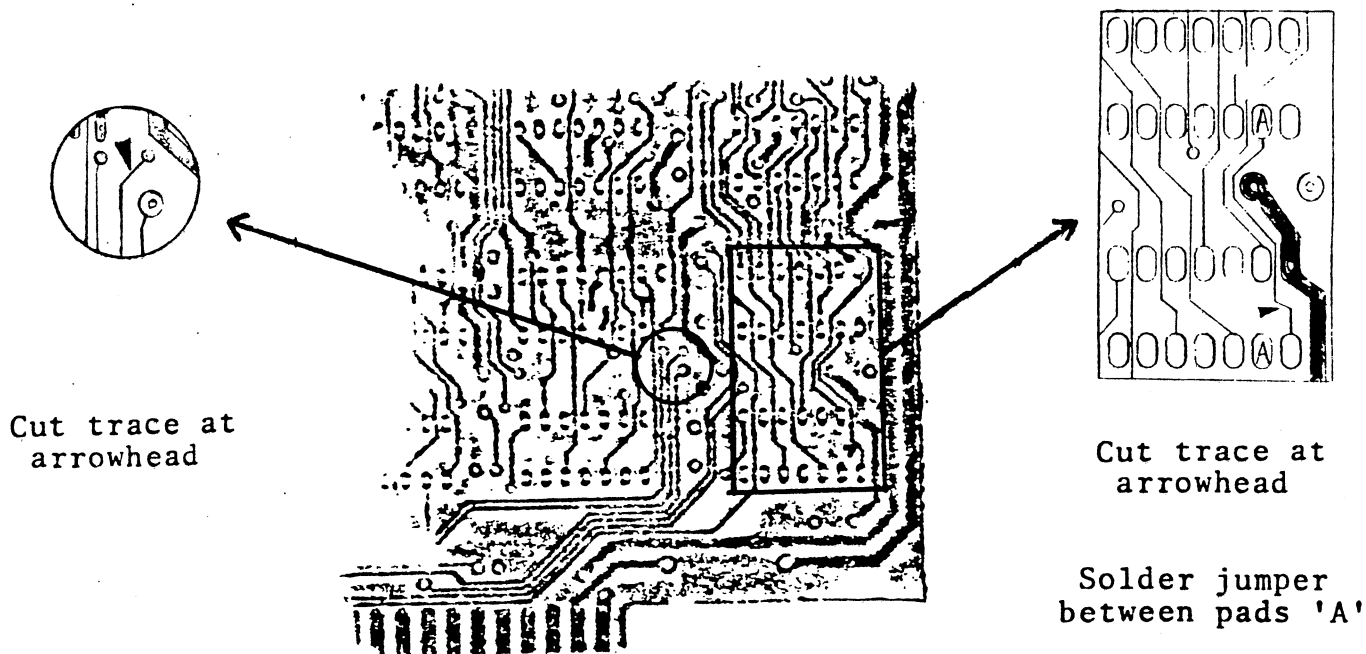
The Betsi board contains refresh control circuitry which allows the SD Sales Dynamic RAM board (EXPANDORAM) to be used with PET/Betsi. Before using this board, the following modifications should be made:

EXPANDORAM Rev. A KITS (See over for Rev. B boards)

1. Remove IC19 and bend pins 8, 9, and 11 outward away from the body.
2. Solder a jumper between IC19 pins 8 and 9.
3. Reinsert IC19 in its socket.

ASSEMBLED Rev. A EXPANDORAMS (assembled EXPANDORAMS purchased from Forethought Products have already been modified as in #1 and #2 below).

1. Cut the two traces on the back side of the EXPANDORAM board as shown below.
2. Solder a short jumper from IC24-9 to IC19-9 as shown.



The EXPANDORAM should be jumpered for Z80 type refresh (jump E11 to E12, no jumper E10 to E11) and jumper pads E13 and E14 should be left open (unconnected). For use with an 8K PET, place memory chips in banks 1, 2 and 3. Enable these banks at the address switch (U2) by turning switches 2, 3 and 4 ON. Switches in U1 (Write Protect) should be set as follows; 1-4 ON, 5 OFF.

EXPANDORAM Rev. B Modifications (Kit or Assembled)

1. Implement the following jumpers on the Expandoram board.

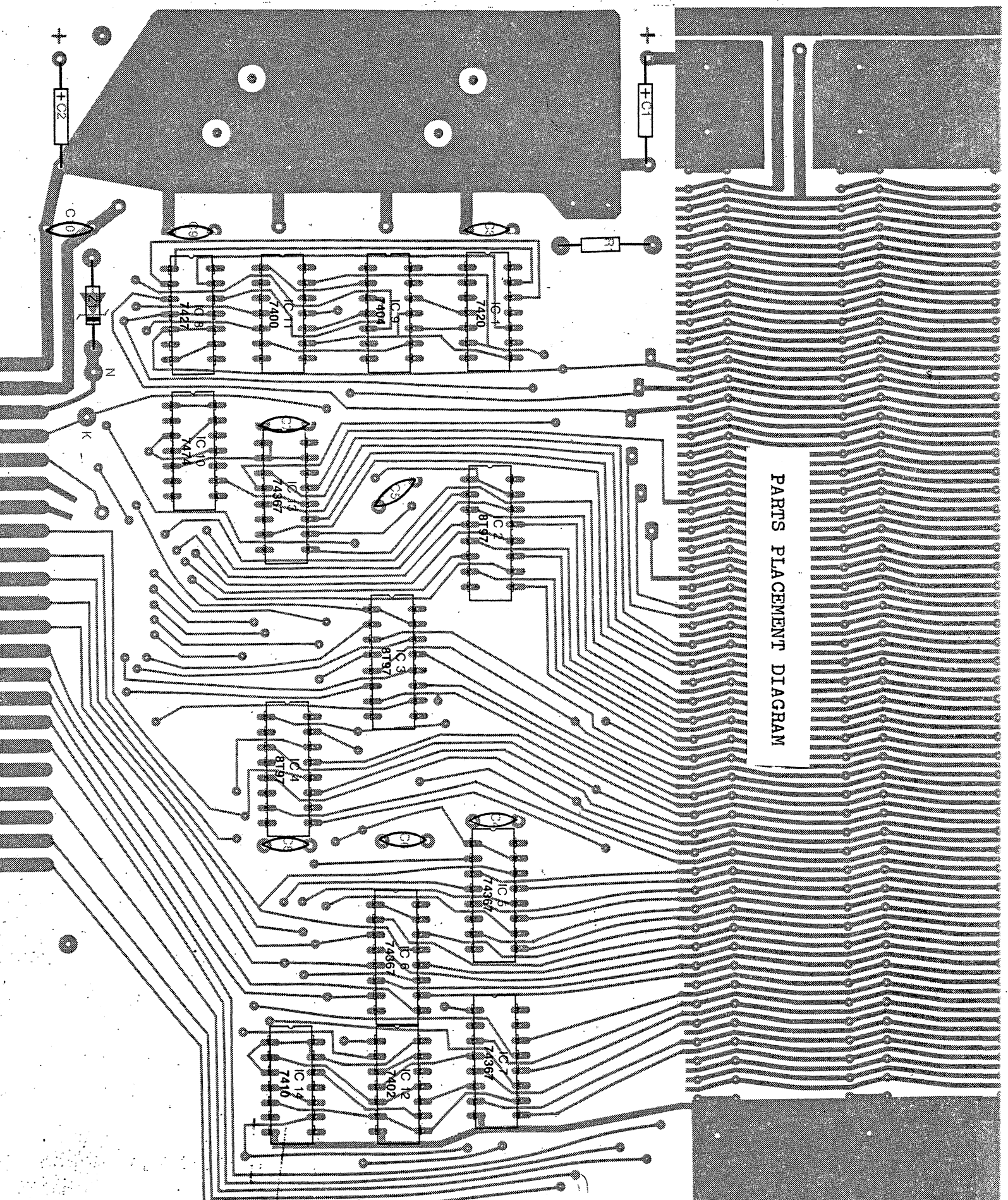
connected	open
E11 to E12	E10
E26 to E27	E25
E19 to E20	E21

2. Remove U19 from its socket, bend pin 11 outward, reinsert the IC.

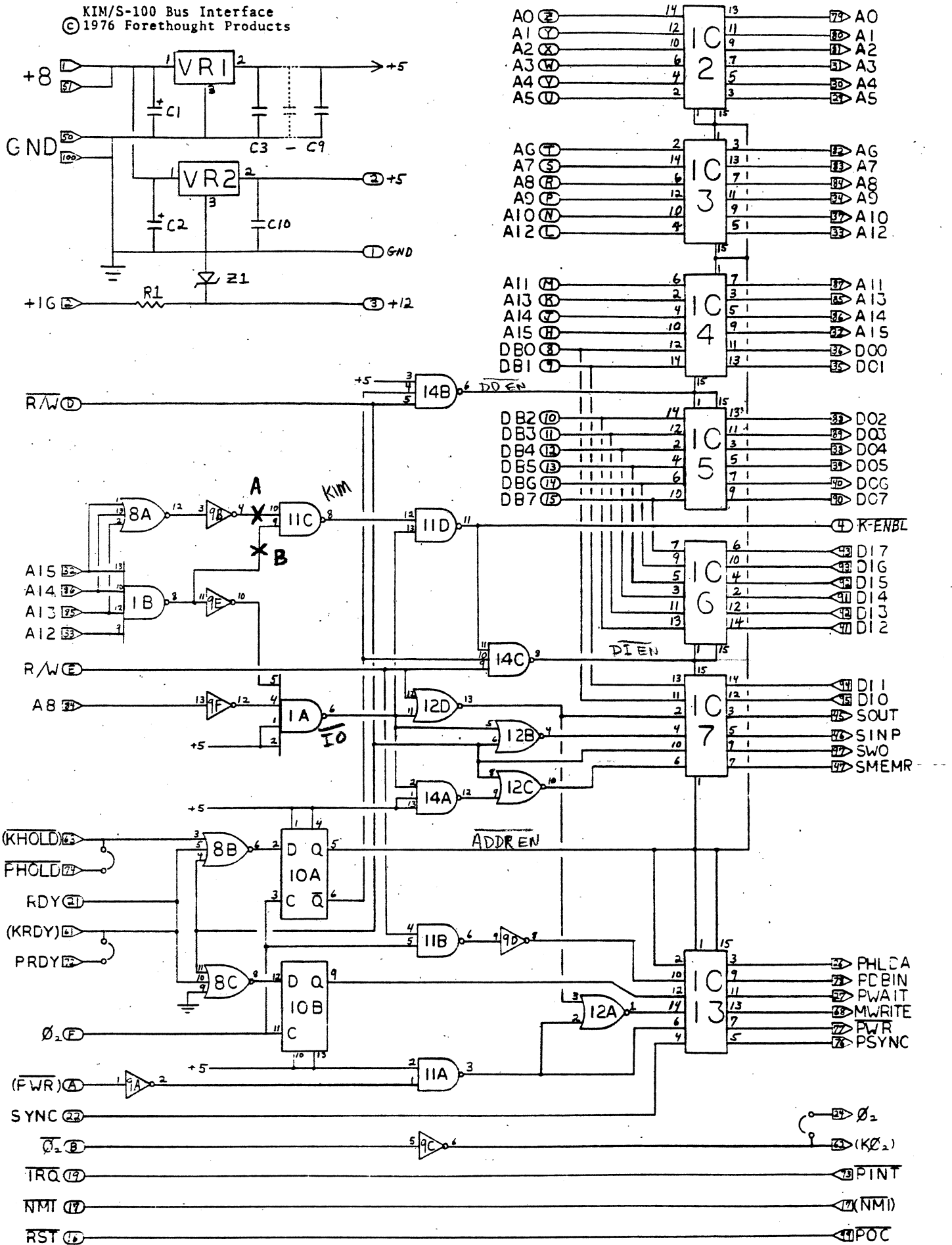
OR

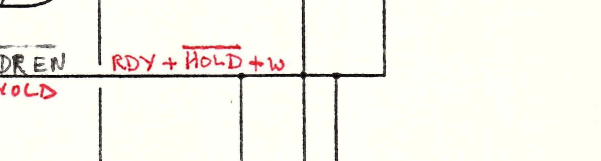
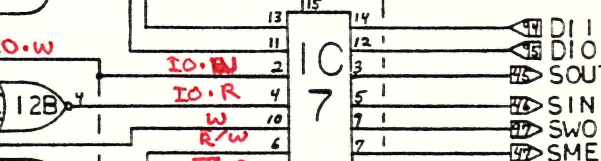
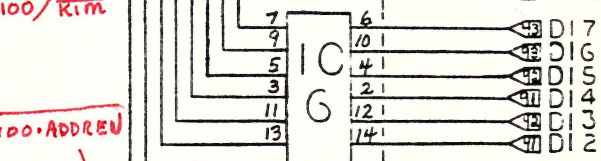
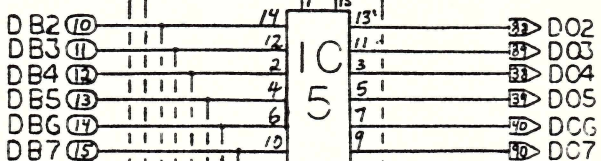
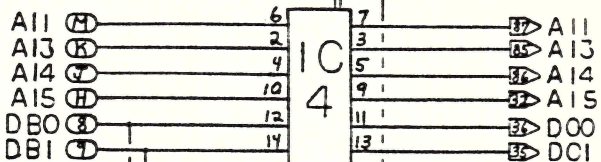
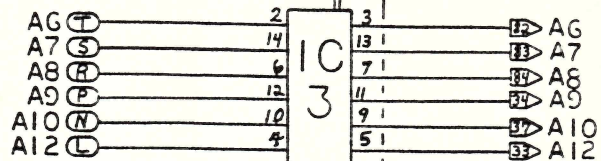
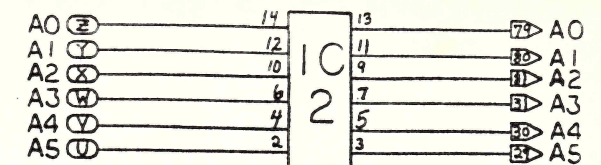
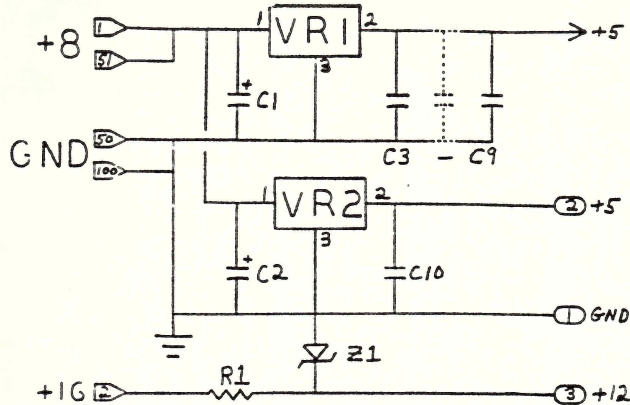
Remove resistor R10 from the board.

PARTS PLACEMENT DIAGRAM

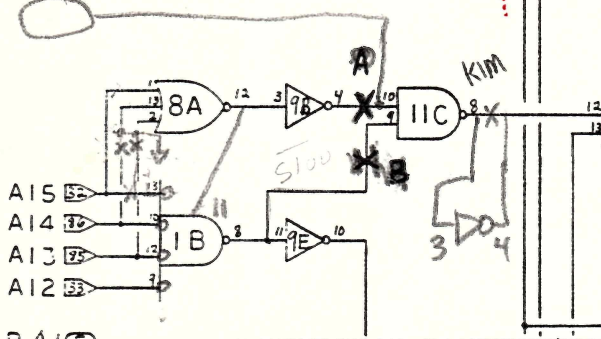


KIM/S-100 Bus Interface
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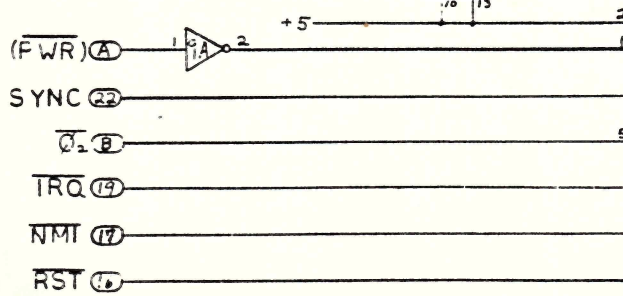
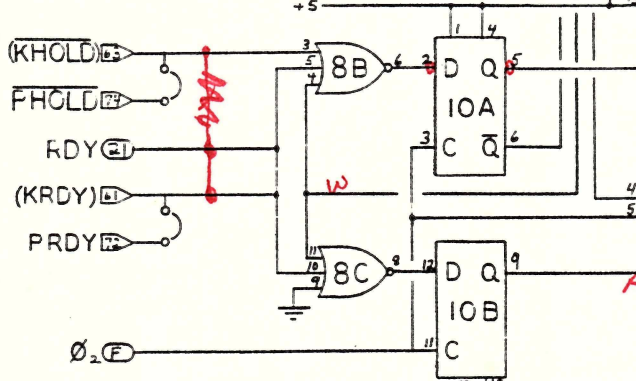




CS8



CS9



ADDR EN · W

S100 / KIM

A · S100 · ADDRESS

IO · W

IO · R

W

R/W

IO · R

ADDR EN

ACK OF HOLD

RDY + HOLD + W

RDY + W

ACK OF WAIT

Φ2 · R/W

Φ2 · W

Φ2 · R/W

Φ2 · W

IO · W · Φ2 · W

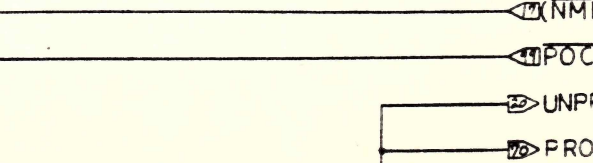
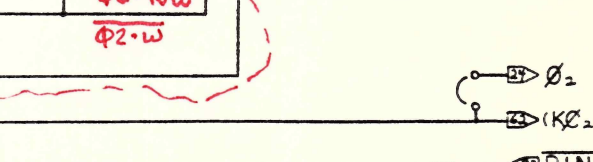
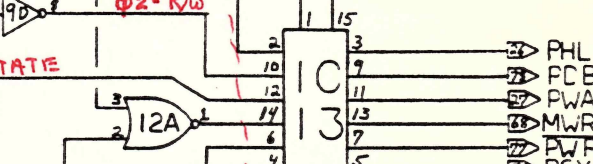
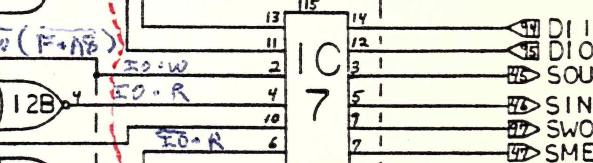
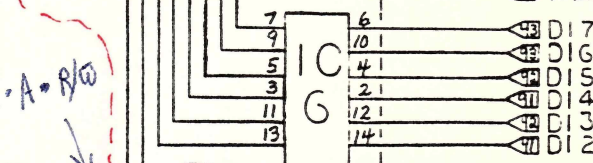
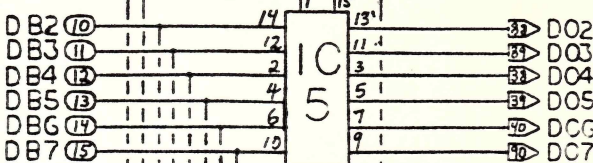
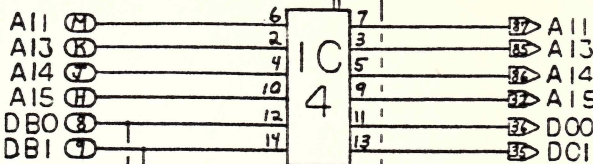
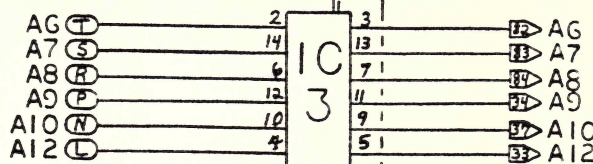
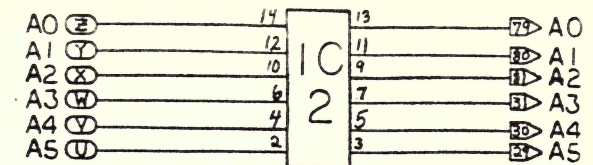
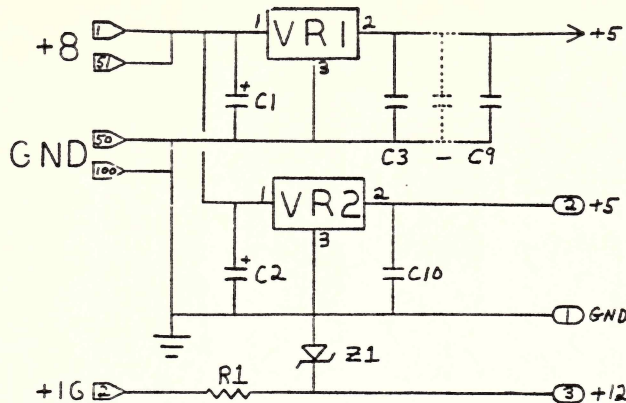
IO · Φ2 · W

Connector Symbols

○ Kimsi edge connector finger

UNPROT

PROT



$$\overline{DO} = A \cdot R/\overline{W}$$

$$\overline{DI} = \overline{K} \cdot A \cdot R/\overline{W}$$

$$AEN = W + RDY + PHOLD$$

$$\overline{A} = ADDRESS$$

$$A = ADDRESS$$

$$\phi 2 \cdot R/\overline{W}$$

$$\phi 2 \cdot \overline{W}$$

$$\phi 2 \cdot R/\overline{W}$$

$$\phi 2 \cdot \overline{W}$$

$$\phi 2 \cdot R/\overline{W}$$

$$\phi 2 \cdot \overline{W}$$

$$\phi 2 \cdot R/\overline{W}$$

$$\phi 2 \cdot \overline{W}$$

$$\phi 2 \cdot R/\overline{W}$$

$$\phi 2 \cdot \overline{W}$$

Connector Symbols

○ Kimsi edge connector finger

UNPROT

PROT

00

$$Z16 \quad 12 \rightarrow 13$$

$$Z13 \quad 11 \rightarrow 13$$

$$13 \rightarrow 12$$

$$11 \rightarrow 10$$

$$9 \rightarrow 8$$

0 - AIM

1 - S100 I/O

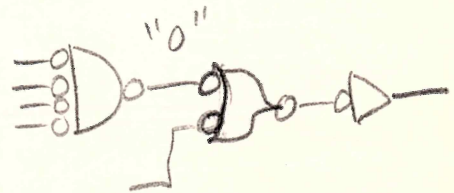
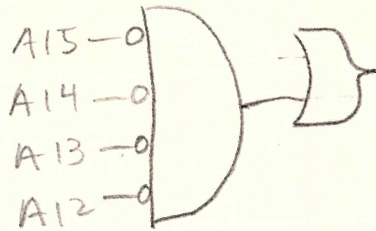
2 - S100

1 -

7 -

8 -

9 - S100



$$(CS0 + A15) + CS8 + CS9$$

$$A15 \cdot A14 \cdot A13 \cdot A12 + A15 \cdot (A14 + A13)$$

